AXIe: AdvancedTCA® Extensions for Instrumentation and Test

November 2012

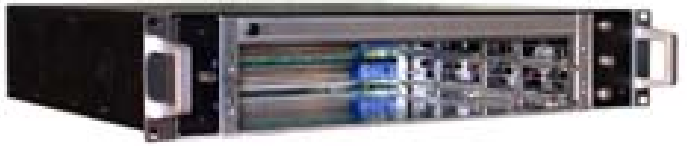
AXIe Specifications: What and Why

- What is it?
  - A family of next-generation, open specifications that extends Advanced Telecom Computing Architecture (AdvancedTCA®) for general purpose instrumentation and semiconductor test
- Why another modular test standard?
  - Lowers cost
    - Highest performance per rack inch
    - Superb scalability
  - Integrates easily with PXI, LXI and IVI
  - Modularity, Flexibility, Speed => addresses a range of platforms
    - Bench top
    - Modular systems
    - ATE Systems

Why AdvancedTCA as a foundation?

- AdvancedTCA PICMG® 3.0 Specification: *proven* open system architecture
- Large board size
  - Ideal for high performance instrumentation
  - Board size matches that of planar instrument design
  - Exceptional cooling
- Rack space efficiency
  - Horizontal and vertical configurations
- Scalability
  - 1 slot to 16 slots, 1 Chassis to many, PXI/PCI adapters
- Ideal for high power applications
  - Single rail power management and robust cooling
- Virtual LXI and PXI
  - Base fabric support of LAN, data fabric support of PCIe
- Robust system management
  - Intelligent Platform Management Interface (IPMI) enables both single chassis and multi-chassis system control functions
- Extensions for I/O allow Zone 3 definitions for identified vertical markets

AdvancedTCA Shelf (Chassis)

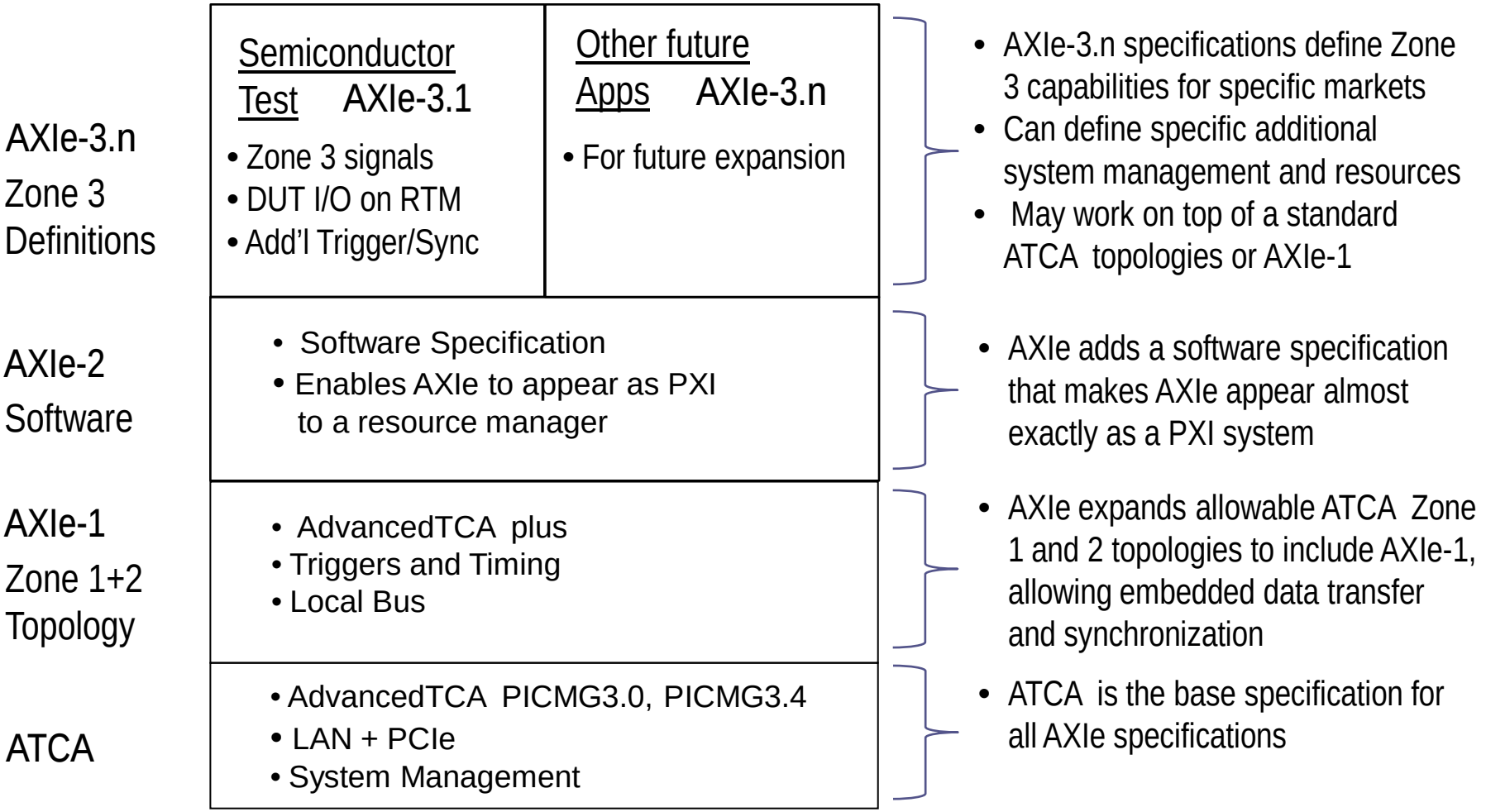


- 2-16 Slot Shelf
  - 2-14 Slots in 19” Rack
- 2 Hub Slots
- 14 Node Slots
- User Zone 3 Backplane

- LAN routed to every slot
- PICMG 3.4: PCIe to every slot
- Large form factor cards
- Flexible power (48V) and air cooled design

AXIe Specification Structure

AXIe is a scalable family of specifications allowing a portfolio of applications.



AXIe 1.0 and 3.1 Features

Feature	1.0	3.1
PCIe & LAN Hubs	x	
Local Bus	x	
Trigger Bus (TRIG)	x	
Frequency Reference (CLK100) & Sync (SYNC)	x	
Star Trigger (STRIG)	x	
Bidirectional DSTAR (4)		x
User Defined Synchronization Signals		x
Load Board Support		x
Field Calibration Support		x

AXIe leverages ATCA

AXIe

AdvancedTCA

- AdvancedTCA specific extensions
- IPMI and resource management
- Timing and Sync
- Zone 3 configurations

…draws from and works with existing instrument standards

PXI

- Virtual PXIe instruments
- PCIe communication

IVI

- Standard drivers work in all Application Development Environments
- VISA specifications

LXI

- Virtual LXI instruments
- LAN communication

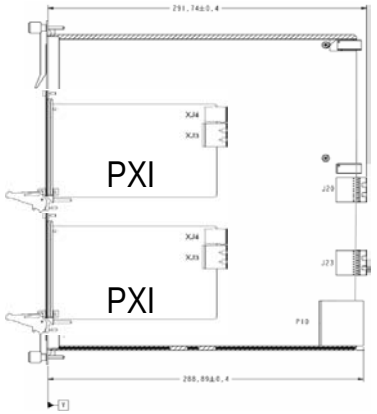
High scalability of AXIe

14 slot Vertical

n U Horizontal

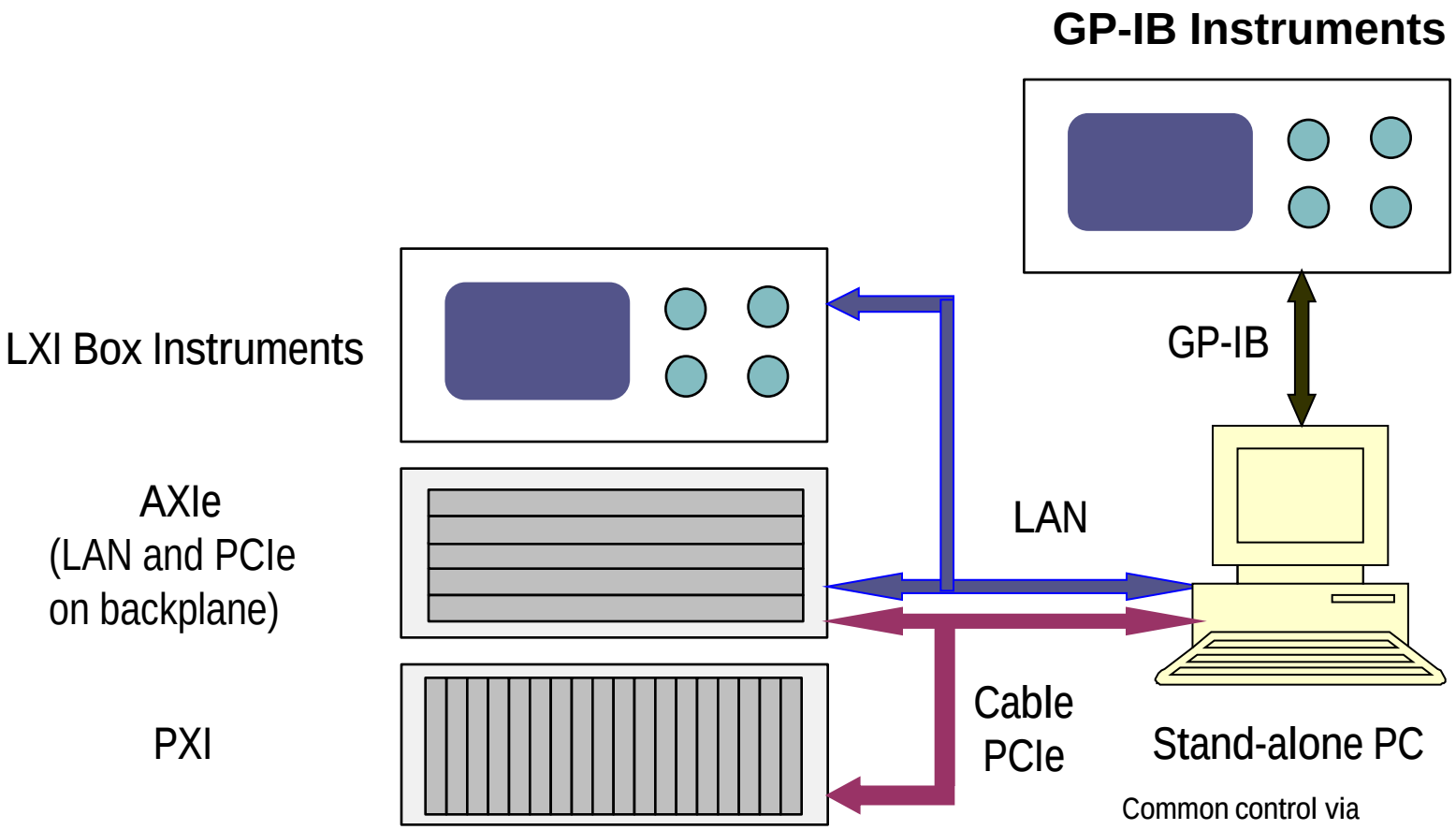
1U

Specialty instrument with AXIe module



PXI carrier module

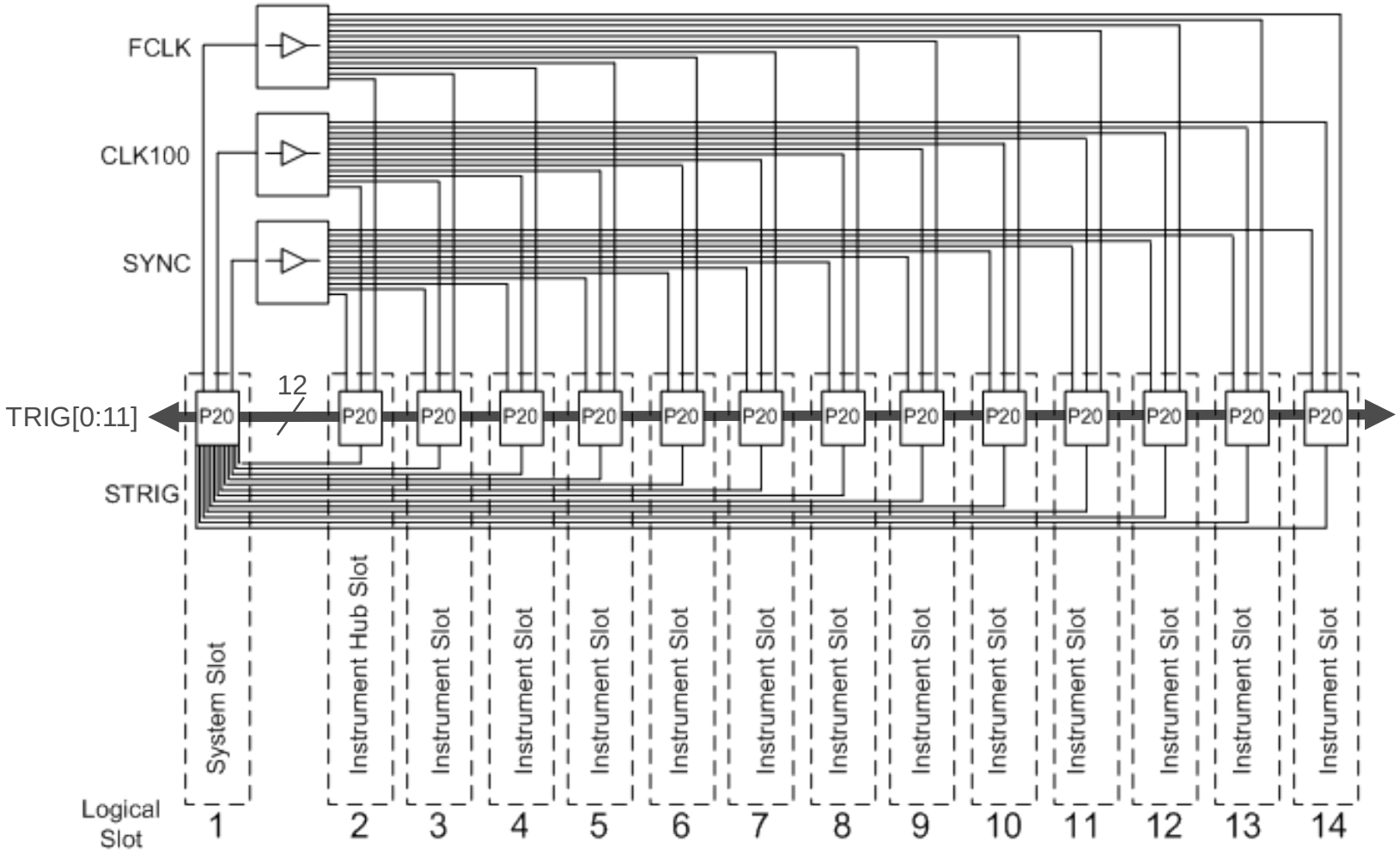
AXIe integration with Rack and Stack



Common control via
- Rack mounted controller, or
- Embedded controller in chassis, or
- Desktop controller

Note: Graphic for example only, instruments do not need to be co-located in same rack unit.

AXIe 1.0 adds Timing and Triggering to ATCA

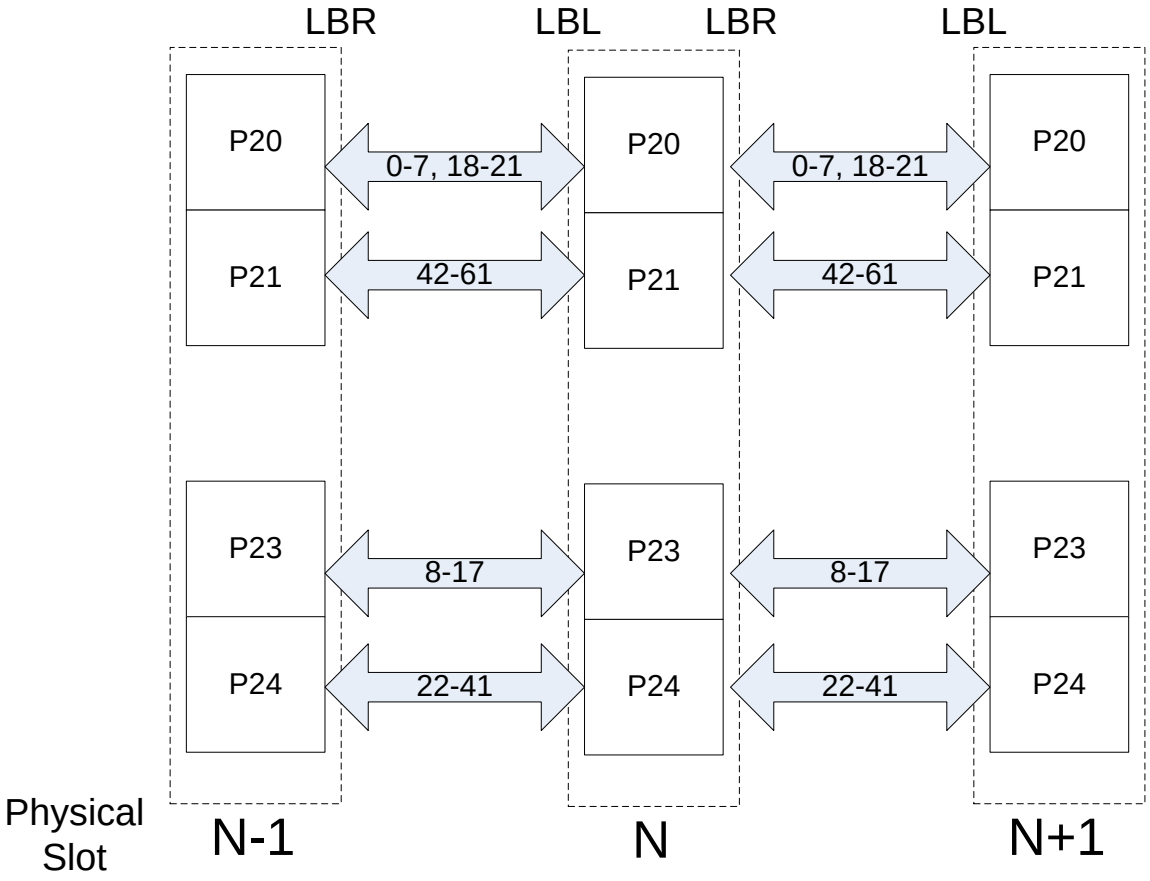


AXIe Performance: Timing and Triggering

RMS Jitter of 12ps has been demonstrated

Slot-to-slot time matching is specified <100ps

AXIe 1.0 adds a High-Speed Local Bus to ATCA



62 x 10Gbps = 620Gbps

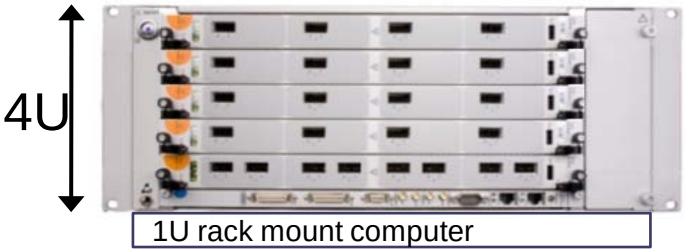
AXIe is the “Big Brother” of PXI

Feature	AXIe	PXIe
Chassis base	AdvancedTCA	cPCI/cPCIe
PCIe maximum data bandwidth (Maximum Gen 2.0): Single peripheral slot to backplane All peripheral slots to system slot	 2 GB/s 26 GB/s	 4 GB/s 8 GB/s
PCIe fabric	Yes	Yes
LAN backplane	Yes	No
Local bus	18 pairs req 62 pairs opt	1 line (13 PXI)
Triggers	Bidirectional Star Trigger 12 signal MLVDS bus	Star Trigger(1xTTL, 3x Diff per slot) 8 Signal TTL bus
Frequency Reference & Sync	100MHz, yes	10MHz, 100MHz, yes
Power per slot	200 W	30 W
Board space per slot (higher density, flexibility)	900 cm^2	160 cm^2
Modules available	New	~1100

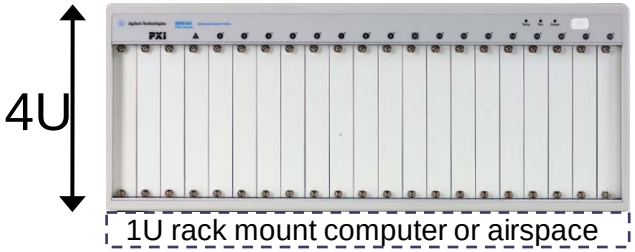
Horizontal AXIe compared with PXI

The tale of two 4U chassis:

AXIe



PXIe



Total module board area	5 x 900 = 4500 cm^2	17 x 160 = 2720 cm^2
Total module volume	4500 x 3 = 13500 cm^3	2720 x 2 = 5440 cm^3
Total module power	200W x 5 = 1000 W	17 x 30 = 510 W

AXIe 3.1 Vision

- Provide an instrumentation environment that reduces the overall cost of test for the Semiconductor Product Test Process.
- Bridge the gap between Device Characterization and high volume Production Test
- Provide Semiconductor ATE instrumentation for Device Characterization
  - High Speed Digital Pins
  - DC & Power Instrumentation

AXIe 3.1 Semiconductor Test Requirements

- Mass Terminated instrument IO mating
  - Managed device test fixtures with quick disconnect
- In Situ system maintenance Diagnostics and Calibration.
  - System Checkers
  - Field Calibration
- High Channel Count Instrumentation
  - 1000's of digital pins
  - 100's of DC power supplies
- Support for single site Characterization AND high volume Multi-Site production

AXIe 3.1 Extensions

- Timing and Triggering Extension
  - Quad Bi-Directional Star Trigger to Each Slot
  - Digital Channel Vender-Defined Synchronization
- Test Fixture Support
  - Instrument I/O via Rear Transition Modules
  - DUT Load Board
  - Modular Checker Load Boards
  - Instrument Calibration Load Boards
- Field Calibration Path
  - External NIST traceable instruments
  - 4 Wire Kelvin Calibration Bus to each slot
  - 1 Amp, 300 Volt Max

AXIe 3.1 Synchronization

- Instrument Triggering
  - 4 Star Triggers from System Module to each Instrument node
  - Non blocking Bi-directional Differential Terminated BLVDS
  - Single Source to Many destinations
  - Chassis to Chassis synchronization via System Module
- Pattern Based Synchronization: UserSync
  - 5 star-distributed signals from System Module to each Instrument node for Pattern Based Synchronization
  - Digital Pattern Synchronization between Digital Instruments and Analog Instruments.
  - Up to 4 Synchronized Chassis

Summary

- Extending AdvancedTCA
  - AXIe is based on AdvancedTCA with extensions for instrumentation and test.
- General Purpose (1.0) , Base Software Specification (2.0), & Semiconductor Test (3.1)
  - AXIe will have a base architecture specification of AXIe 1.0 for general instrumentation, a base software specification, AXIe 2.0, and a Zone 3 specification AXIe 3.1 for semiconductor test.
- More Performance, Scalability, Flexibility
  - AXIe delivers higher performance in a flexible, scalable platform.
- PXI, LXI, IVI
  - AXIe works well with other standards, such as PXI, LXI and IVI.

    AXIe is the “Big Brother” of PXI
- Specifications may be downloaded from the AXIe Consortium website at www.axiestandard.org

Specification Management

- AXIe Consortium
  - AXIe Consortium manages AXIe 1.0, 2.0 and 3.1 specifications
  - For more information, go to www.axiestandard.org or email Bob Helsel, Executive Director at execdir@axiestandard.org
- Potential future AXIe standard efforts
  - Improved integration of ATCA, AXIe 1.0, AXIe 2.0 and AXIe 3.1 combinations
  - AXIe 3.N specifications for additional markets
  - Fully integrated PXImc
  - MicroTCA® derivatives for AXIe

* MicroTCA is a registered trademark of the PCI Industrial Computer Manufacturers Group (PICMG)