AXIe: AdvancedTCA® Extensions for Instrumentation and Test
AXIe Specifications: What and Why

- **What is it?**
  - A family of next-generation, open specifications that extends Advanced Telecom Computing Architecture (AdvancedTCA®) for general purpose instrumentation and semiconductor test

- **Why another modular test standard?**
  - Lowers cost
    - Highest performance per rack inch
    - Superb scalability
  - Integrates easily with PXI, LXI and IVI
  - Modularity, Flexibility, Speed => addresses a range of platforms
    - Bench top
    - Modular systems
    - ATE Systems

* AdvancedTCA is a registered trademark of the PCI Industrial Computer Manufacturers Group (PICMG)
Why AdvancedTCA as a foundation?

- **AdvancedTCA PICMG® 3.0 Specification:** proven open system architecture
- **Large board size**
  - Ideal for high performance instrumentation
  - Board size matches that of planar instrument design
  - Exceptional cooling
- **Rack space efficiency**
  - Horizontal and vertical configurations
- **Scalability**
  - 1 slot to 16 slots, 1 Chassis to many, PXI/PCI adapters
- **Ideal for high power applications**
  - Single rail power management and robust cooling
- **Virtual LXI and PXI**
  - Base fabric support of LAN, data fabric support of PCIe
- **Robust system management**
  - Intelligent Platform Management Interface (IPMI) enables both single chassis and multi-chassis system control functions
- **Extensions** for I/O allow Zone 3 definitions for identified vertical markets

* PICMG is a registered trademark of the PCI Industrial Computer Manufacturers Group.*
Advanced TCA Shelf (Chassis)

- 2-16 Slot Shelf
  - 2-14 Slots in 19” Rack
- 2 Hub Slots
- 14 Node Slots
- User Zone 3 Backplane
- LAN routed to every slot
- PICMG 3.4: PCIe to every slot
- Large form factor cards
- Flexible power (48V) and air cooled design
## AXIe Specification Structure

AXIe is a scalable family of specifications allowing a portfolio of applications.

<table>
<thead>
<tr>
<th>Zone 3</th>
<th>Zone 1+2 Topology</th>
<th>ATCA</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Semiconductor Test</strong></td>
<td><strong>AXIe 1.0</strong></td>
<td><strong>AXIe 3.1</strong></td>
</tr>
<tr>
<td>AXIe 3.1</td>
<td>ATCA + Core Triggers, Timing and Local bus</td>
<td>• Zone 3 signals</td>
</tr>
<tr>
<td>• Zone 3 signals</td>
<td></td>
<td>• DUT I/O on RTM</td>
</tr>
<tr>
<td>• DUT I/O on RTM</td>
<td>• Add’l Trigger/Sync</td>
<td>• Analog Busses</td>
</tr>
<tr>
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<td>• FRU &amp; RTM Management</td>
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</tr>
<tr>
<td>• Analog Busses</td>
<td></td>
<td>• AXIe 3.N specifications define Zone 3 capabilities for specific markets</td>
</tr>
<tr>
<td>• FRU &amp; RTM Management</td>
<td></td>
<td>• Can define specific additional system management and system resources.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• May work on top of a standard ATCA topologies or AXIe 1.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• AXIe expands on the spectrum of allowable ATCA Zone 1 and 2 topologies to include AXIe 1.0, allowing embedded data transfer and synchronization enhancements</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• ATCA is the base specification for all AXIe specifications</td>
</tr>
</tbody>
</table>

### Other future Apps

<table>
<thead>
<tr>
<th>AXIe 3.N</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Examples:</td>
</tr>
<tr>
<td>• Network Test</td>
</tr>
<tr>
<td>• Physics</td>
</tr>
<tr>
<td>• Liquid Cooling</td>
</tr>
<tr>
<td>• Custom</td>
</tr>
</tbody>
</table>

### AXIe Specification Structure

- **AXIe** is a scalable family of specifications allowing a portfolio of applications.
- **ATCA** is the base specification for all AXIe specifications.
# AXle 1.0 and 3.1 Features

<table>
<thead>
<tr>
<th>Feature</th>
<th>1.0</th>
<th>3.1</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCIe &amp; LAN Hubs</td>
<td>x</td>
<td></td>
</tr>
<tr>
<td>Local Bus</td>
<td>x</td>
<td></td>
</tr>
<tr>
<td>Trigger Bus (TRIG)</td>
<td>x</td>
<td></td>
</tr>
<tr>
<td>Frequency Reference (CLK100) &amp; Sync (SYNC)</td>
<td>x</td>
<td></td>
</tr>
<tr>
<td>Star Trigger (STRIG)</td>
<td>x</td>
<td></td>
</tr>
<tr>
<td>Bidirectional DSTAR (4)</td>
<td></td>
<td>x</td>
</tr>
<tr>
<td>User Defined Synchronization Signals</td>
<td></td>
<td>x</td>
</tr>
<tr>
<td>Load Board Support</td>
<td></td>
<td>x</td>
</tr>
<tr>
<td>Field Calibration Support</td>
<td></td>
<td>x</td>
</tr>
</tbody>
</table>
AXIe leverages ATCA

...draws from and works with existing instrument standards

AXIe
- AdvancedTCA specific extensions
- IPMI and resource management
- Timing and Sync
- Zone 3 configurations

AdvancedTCA

PXI
- Virtual PXIe instruments
- PCIe communication

IVI
- Standard drivers work in all Application Development Environments
- VISA specifications

LXI
- Virtual LXI instruments
- LAN communication
High scalability of AXIe

Specialty instrument with AXIe module

1U

n U Horizontal

14 slot Vertical

PXI carrier module
AXIe integration with Rack and Stack

Note: Graphic for example only, instruments do not need to be co-located in same rack unit.
AXIe 1.0 adds Timing and Triggering to ATCA
AXIe Performance: Timing and Triggering

RMS Jitter of 12ps has been demonstrated

Slot-to-slot time matching is specified <100ps
AXIe 1.0 adds a High-Speed Local Bus to ATCA

62 x 10Gbps = 620Gbps
### AXIe is the “Big Brother” of PXI

<table>
<thead>
<tr>
<th>Feature</th>
<th>AXIe</th>
<th>PXIe</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chassis base</td>
<td>AdvancedTCA</td>
<td>cPCI/cPCIe</td>
</tr>
<tr>
<td>PCIe maximum data bandwidth (Maximum Gen 2.0):</td>
<td>2 GB/s</td>
<td>4 GB/s</td>
</tr>
<tr>
<td>Single peripheral slot to backplane</td>
<td>26 GB/s</td>
<td>8 GB/s</td>
</tr>
<tr>
<td>All peripheral slots to system slot</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PCIe fabric</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>LAN backplane</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Local bus</td>
<td>18 pairs req</td>
<td>1 line (13 PXI)</td>
</tr>
<tr>
<td></td>
<td>62 pairs opt</td>
<td></td>
</tr>
<tr>
<td>Triggers</td>
<td>Bidirectional Star</td>
<td>Star Trigger(1xTTL, 3x</td>
</tr>
<tr>
<td></td>
<td>Trigger 12 signal MLVDS</td>
<td>Diff per slot)</td>
</tr>
<tr>
<td></td>
<td>bus</td>
<td>8 Signal TTL bus</td>
</tr>
<tr>
<td>Frequency Reference &amp; Sync</td>
<td>100MHz, yes</td>
<td>10MHz, 100MHz, yes</td>
</tr>
<tr>
<td>Power per slot</td>
<td>200 W</td>
<td>30 W</td>
</tr>
<tr>
<td>Board space per slot (higher density, flexibility)</td>
<td>900 cm²</td>
<td>160 cm²</td>
</tr>
<tr>
<td>Modules available</td>
<td>New</td>
<td>~1100</td>
</tr>
</tbody>
</table>
Horizontal AXIe compared with PXI

The tale of two 4U chassis:

<table>
<thead>
<tr>
<th>AXIe</th>
<th>PXIe</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total module board area</td>
<td>5 x 900 = 4500 cm²</td>
</tr>
<tr>
<td>Total module volume</td>
<td>4500 x 3 = 13500 cm³</td>
</tr>
<tr>
<td>Total module power</td>
<td>200W x 5 = 1000 W</td>
</tr>
<tr>
<td></td>
<td>17 x 160 = 2720 cm²</td>
</tr>
<tr>
<td></td>
<td>2720 x 2 = 5440 cm³</td>
</tr>
<tr>
<td></td>
<td>17 x 30 = 510 W</td>
</tr>
</tbody>
</table>
AXle 3.1 Vision

- Provide an instrumentation environment that reduces the overall cost of test for the Semiconductor Product Test Process.
- Bridge the gap between Device Characterization and high volume Production Test
- Provide Semiconductor ATE instrumentation for Device Characterization
  - High Speed Digital Pins
  - DC & Power Instrumentation
AXIe 3.1 Semiconductor Test Requirements

- Mass Terminated instrument IO mating
  - Managed device test fixtures with quick disconnect
- In Situ system maintenance Diagnostics and Calibration.
  - System Checkers
  - Field Calibration
- High Channel Count Instrumentation
  - 1000’s of digital pins
  - 100’s of DC power supplies
- Support for single site Characterization AND high volume Multi-Site production
AXIe 3.1 Extensions

• Timing and Triggering Extension
  ▫ Quad Bi-Directional Star Trigger to Each Slot
  ▫ Digital Channel Vendor-Defined Synchronization

• Test Fixture Support
  ▫ Instrument I/O via Rear Transition Modules
  ▫ DUT Load Board
  ▫ Modular Checker Load Boards
  ▫ Instrument Calibration Load Boards

• Field Calibration Path
  ▫ External NIST traceable instruments
  ▫ 4 Wire Kelvin Calibration Bus to each slot
  ▫ 1 Amp, 300 Volt Max
AXIe 3.1 Synchronization

- Instrument Triggering
  - 4 Star Triggers from System Module to each Instrument node
  - Non blocking Bi-directional Differential Terminated BLVDS
  - Single Source to Many destinations
  - Chassis to Chassis synchronization via System Module

- Pattern Based Synchronization: UserSync
  - 5 star-distributed signals from System Module to each Instrument node for Pattern Based Synchronization
  - Digital Pattern Synchronization between Digital Instruments and Analog Instruments.
  - Up to 4 Synchronized Chassis
Summary

- Extending AdvancedTCA
  - AXIe is based on AdvancedTCA with extensions for instrumentation and test.

- General Purpose (1.0) & Semiconductor Test (3.1)
  - AXIe will have a base architecture specification of AXIe 1.0 for general instrumentation, and a Zone 3 specification AXIe 3.1 for semiconductor test.

- More Performance, Scalability, Flexibility
  - AXIe delivers higher performance in a flexible, scalable platform.

- PXI, LXI, IVI
  - AXIe works well with other standards, such as PXI, LXI and IVI.

AXIe is the “Big Brother” of PXI

- Specifications may be downloaded from the AXIe Consortium website at www.axiestandard.org
Specification Management

• AXIe Consortium
  ▫ AXIe Consortium manages AXIe 1.0 and 3.1 specifications
  ▫ For more information, go to www.axiestandard.org or email Bob Helsel, Executive Director at execdir@axiestandard.org

• Potential future AXIe standard efforts
  ▫ Improved integration of ATCA, AXIe 1.0, and AXIe 3.1 combinations
  ▫ AXIe 2.0 software specification
  ▫ AXIe 3.N specifications for additional markets
  ▫ Fully integrated PXImc
  ▫ MicroTCA® derivatives for AXIe

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