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Important Information ............................................................................... 2

Warranty 2

Trademarks 2

Architecture Specification ........................................................................... 5

1. Overview of the Specification .............................................................. 6
   1.1 Introduction ..................................................................................... 6
   1.2 Intended Audience and Scope of the Specification ......................... 6
   1.3 Terminology .................................................................................. 6
   1.4 Organization of Specification .......................................................... 7
   1.5 Signal Naming Conventions ............................................................. 8
   1.6 Useful Web Sites ........................................................................... 8
   1.7 Architecture Overview .................................................................. 8
      1.7.1 Mechanical Architecture Overview ......................................... 8
      1.7.2 Electrical Architecture Overview .............................................. 9
      1.7.2.1 System and Instrument Slots ................................................ 9
      1.7.2.2 Backplane Identification ..................................................... 9
      1.7.2.3 System Slot Overview .......................................................... 9
      1.7.2.4 Instrument Slot Overview ..................................................... 10
      1.7.2.5 Zone 3 Backplane Connectors .............................................. 11
      1.7.2.6 Triggers and Synchronization ............................................... 11
      1.7.2.7 Interoperability with AXIe 1.0 and ATCA® PCMIG® 3.0 ....... 12
   1.8 Conformance Requirements ............................................................. 12
   1.9 References ................................................................................... 12

2. Mechanical Requirements .................................................................... 13
   2.1 Drawing Standard ......................................................................... 13
   2.2 Dimensional Units ....................................................................... 13
   2.3 Zone 3 Backplane Interface ............................................................ 13
      2.3.1 Minimum Number of Slots .................................................... 13
      2.3.2 Maximum Number of Slots .................................................... 13
      2.3.3 Slot Location ......................................................................... 13
      2.3.4 Slot Numbering ..................................................................... 13
      2.3.5 Backplane Dimensions .......................................................... 13
      2.3.6 Zone 3 Backplane Connector Requirements ......................... 14
         2.3.6.1 Backplane Connector Locations .................................... 14
         2.3.6.2 Mechanical Alignment and Keying .................................. 14
         2.3.6.3 System Slot ................................................................. 16

AXIe Consortium 3 AXIe 3.1: Semiconductor Test Extension Rev 1.0
3. Electrical Requirements ................................................................. 20

3.1 Control Signals .................................................................................. 20
  3.1.1 Reset Signal Requirements ................................................................ 20
    3.1.1.1 Backplane Requirements ................................................................. 20
    3.1.1.2 Module Requirements ...................................................................... 20
  3.1.2 DUT Power On Signal Requirements .................................................. 20
    3.1.2.1 Backplane Requirements ................................................................. 20
    3.1.2.2 Module Requirements ...................................................................... 20
  3.1.3 Reserved Signal Requirements ............................................................ 21
    3.1.3.1 Backplane Requirements ................................................................. 21
    3.1.3.2 Module Requirements ...................................................................... 21

3.2 Analog and Calibration Bus Signals ...................................................... 22
  3.2.1 Analog Bus Interface Requirements .................................................... 23
    3.2.1.1 Backplane Requirements ................................................................. 23
    3.2.1.2 System Module Requirements .......................................................... 23
    3.2.1.3 Instrument Module Requirements ..................................................... 23
  3.2.2 Calibration Bus Interface Requirements .............................................. 24
    3.2.2.1 Backplane Requirements ................................................................. 24
    3.2.2.2 System Module Requirements .......................................................... 24
    3.2.2.3 Instrument Module Requirements ..................................................... 24

3.3 Star Trigger Signals ............................................................................ 24
  3.3.1 Backplane Requirements .................................................................... 24
  3.3.2 System Module Requirements ............................................................. 25
  3.3.3 Instrument Module Requirements ........................................................ 26

3.4 Star User Signals .................................................................................. 26
  3.4.1 Backplane Requirements .................................................................... 27
  3.4.2 System Module Requirements ............................................................. 27
  3.4.3 Instrument Module Requirements ........................................................ 28

3.5 DUT Signals ....................................................................................... 28
  3.5.1 DUT I/O Interface Signal Requirements .............................................. 28
    3.5.1.1 Backplane Requirements ................................................................. 28
    3.5.1.2 Module Requirements ...................................................................... 28
  3.5.2 DUT Power Supply Requirements ....................................................... 29
    3.5.2.1 Backplane Requirements ................................................................. 29
    3.5.2.2 System Module Requirements .......................................................... 29
  3.5.3 IPMI I²C FRU Identification Requirements ...................................... 29
    3.5.3.1 Backplane Requirements ................................................................. 29
    3.5.3.2 System Module and Instrument Module Requirements ..................... 30
  3.5.4 I²C User Interface Requirements ....................................................... 30
    3.5.4.1 Backplane Requirements ................................................................. 30
    3.5.4.2 System and Instrument Module Requirements .................................... 30

3.6 Zone 3 Backplane Connector Pin-Out and Signal Assignment ................ 32
  3.6.1 System Slot Pin Assignments .............................................................. 32
  3.6.2 Instrument Slot Pin Assignments ......................................................... 34
This section is an overview of the revision history of the AXIe 3.1 specification.

### Architecture Specification Revisions

<table>
<thead>
<tr>
<th>Revision Number</th>
<th>Date of Revision</th>
<th>Revision Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>June 30, 2010</td>
<td>Approved and Released</td>
</tr>
</tbody>
</table>
1. Overview of the Specification

1.1 Introduction

This section summarizes the AXIe 3.1 Semiconductor Test Extension Specification itself and contains general information that the reader may need in order to understand, interpret, and implement aspects of this specification. These aspects include the following:
- Intended Audience
- Terminology
- Organization of the specification
- Signal naming conventions
- Links to useful web sites
- Architecture Overview
- Conformance Requirements
- References
- Mechanical and Electrical Architecture Requirements

1.2 Intended Audience and Scope of the Specification

This specification is primarily for the use of AXIe equipment manufacturers and system integrators who are implementing products and systems that conform to the requirements of this specification. The primary audience is assumed to have extensive knowledge of modular measurement hardware architectures, and access to the various referenced technical specifications. However, this specification should also prove useful to managers and anyone else involved in the selection of modular test system platforms and architectures.

1.3 Terminology

AXIe terminology is modeled largely on language familiar to manufacturers, system integrators, and end users in the test and measurement industry. In many cases this is different from the telecom-derived terminology used in the AdvancedTCA® specification.

Here are the definitions of some of the more common AXIe terms used within this document:

- **ATCA®** - Advanced Telecom Computing Architecture.
- **Chassis** - This is the primary AXIe infrastructure component that hosts AXIe modules. A typical AXIe chassis includes a backplane, subrack, power supply(ies), fan tray(s), shelf manager, and sheet metal enclosure. It may include rack mounting provisions. A chassis may also include an embedded system module. (See Integrated Chassis.)
- **DSTAR<A..D>** - Differential Star Distributed signals A thru D: Typically used for triggering Instrument Modules to other Instrument Modules via the System Module.
- **DUT** - Device Under Test.
- **DUT I/O** - Device Under Test Input/Output signals.
- **DUT Load Board** – A printed circuit board designed as an interface circuit between the automatic test equipment and the device under test.
- **EEPROM** - Electrical Erasable programmable read only memory: A non-volatile device that retains its contents even when the power is turned off.
- **FRU** - Field Replaceable Unit: A generic term used to describe any hardware device, or more commonly a part or component of a device or system, which easily can be replaced by a skilled technician without having to send the entire device or system to be repaired.
- **I²C** - Inter-IC (also known as I2C): A bi-directional serial bus that provides a communication link between integrated circuits.
- **Integrated Chassis** - An AXIe chassis that has built-in system module functionality in lieu of an AXIe-standard system slot.
- **IPMB** - Intelligent Platform Management Bus: A bus based on the I²C interface and is part of the IMPI architecture.
- **IPMI** - Intelligent Platform Management Interface: An infrastructure that provides communications, management, and control among the distributed controllers and to an overall system manager.

- **Load Board** - A Load Board is typically a printed circuit board connecting signals from the System and/or Instrument Modules to a common location. A Load Board can be designed for DUT applications, system test or calibration functions or any other applications requiring the connection of system components in a common environment.

- **LVDS** - Low Voltage Differential Signaling: Defined in TIA/EIA-644 LVDS is a point-to-point electrical interface.

- **M-LVDS** - Multi-point Low Voltage Differential Signaling: Defined in TIA/EIA-899. It is a multi drop and multi sourced signaling standard.

- **Module** - A PC assembly, face plate, and enclosure that plugs into an AXIe slot. Equivalent to an AdvancedTCA® front board.

- **PCI Express** - Serialized evolution of PCI.

- **PICMG** - PCI Industrial Computer Manufacturers Group.

- **PXI** - PCI eXtensions for Instrumentation.

- **PXI Express** - PCI Express eXtensions for Instrumentation.

- **RTM** - Rear Transition Module: Used to interconnect System or Instrument Module DUT I/O to the DUT.

- **System Module** - An AXIe module that includes LAN switches, PCIe® switches, system timing and trigger resources, and/or other central resources. A system module installs in a chassis system slot. An AXIe system module is comparable to an AdvancedTCA® hub board.

- **Embedded System Module** - System module functionality that is embedded in an integrated chassis.

- **System Slot** - An AXIe slot that supports a system module. It is always logical slot 1. It is comparable to an AdvancedTCA® hub slot.

- **Instrument Module** - Any AXIe module that is not a system module.

- **VHDM** - Very High Density Metric: A connector system designed for applications requiring high interconnect density and high speed signal integrity.

### 1.4 Organization of Specification

This specification consists of a system of numbered RULES, RECOMMENDATIONS, PERMISSIONS, and OBSERVATIONS, along with supporting text, tables, and figures.

**RULEs** outline the core requirements of the specification. They are characterized by the keyword “SHALL”. Conformance to these rules provides the necessary level of compatibility to support the multi-vendor interoperability expected by system integrators and end users in the test and measurement industry. Products that conform to this specification must meet all of the requirements spelled out in the various rules.

**RECOMMENDATIONs** provide additional guidance that will help AXIe equipment manufacturers improve their users’ experiences with AXIe systems. They are characterized by the keyword “SHOULD”. Following the recommendations should improve the functionality, flexibility, interoperability, and/or usability of AXIe products. Products are not required to implement the recommendations.

**PERMISSIONs** explicitly highlight some of the flexibility of the AXIe specification. They are characterized by the keyword “MAY”. The permissions generally clarify the range of design choices that are available to product and system designers at their discretion. They allow designers to trade off functionality, cost, and other factors in order to produce products that meet their users’ expectations. Permissions are neutral and imply no preference as to their implementation.

**OBSERVATIONs** explicitly highlight some of the important nuances of the specification. They help the readers to fully understand some of the implications of the specification’s requirements and/or the rationale behind particular requirements. They generally provide valuable design guidance.

All rules, recommendations, permissions, and observations must be considered in the context of the surrounding text, tables, and figures. Rules may explicitly or implicitly incorporate information from the text, tables, and figures. Although the authors of this specification have gone to significant effort to insure that all of the necessary requirements are spelled out in the rules, it is possible that some important requirements appear only in the specification’s free text. Conservative design practice dictates that such embedded requirements be treated as rules.
Successful implementation of AXIe products and systems requires in-depth knowledge of the AXIe 1.0 specification, AXIe 3.1 specification, and the AdvancedTCA® specification. This specification does not reproduce any content from the AdvancedTCA® specification.

1.5 Signal Naming Conventions
All signals are active high unless denoted by a trailing # symbol. Differential signals are denoted by a trailing + (positive) or – (negative) symbol.

1.6 Useful Web Sites
Below is a list of Web site links that at the time of publication of this specification point to sites with information useful in the understanding and design of AXIe products:

- [http://www.axiestandard.org](http://www.axiestandard.org) AXIe specifications
- [http://www.pcisig.com/](http://www.pcisig.com/) PCI and PCI Express specifications

1.7 Architecture Overview

1.7.1 Mechanical Architecture Overview
AXIe 3.1 defines a backplane interface for Zone 3 of the AdvancedTCA® specification, subsequently called the ATCA® specification. This large card format provides both more area and greater component height to support high capability digital instrumentation normally only found in proprietary formats. A high performance connector system has been added to support the Test Extensions associated with PXI-Express and are located in the Zone 3 section of the modules. This specification uses different names for the Module and slot types as compared to ATCA®. The table below shows the AXIe 3.1 specification name and the equivalent ATCA® specification name.

<table>
<thead>
<tr>
<th>AXIe 3.1 Specification Name</th>
<th>ATCA® Specification Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>System Module</td>
<td>Hub board</td>
</tr>
<tr>
<td>Instrument Module</td>
<td>Node board</td>
</tr>
</tbody>
</table>

Table 1-1: AXIe 3.1 and ATCA® Specification Names

1.7.1.1 Interoperability with AXIe 1.0 and ATCA® PCMIG® 3.0
The AXIe 3.1 specification defines a Zone 3 backplane as an extension to AXIe 1.0 and ATCA® platforms. This presents interoperability issues with AXIe 1.0 and ATCA® 3.0 modules that do not implement the AXIe 3.1 backplane interface.

Mechanically ATCA® 3.0 modules can use any user defined connectors in the Zone 3 area of the backplane. These user connectors may mechanically interfere with the AXIe 3.1 (VHDM) connectors and may preclude the use of these modules with an AXIe 3.1 backplane.
AXIe 1.0 and some ATCA® 3.0 Modules that do not include a Zone 3 connector may be installed in a chassis having an AXIe 3.1 compatible Zone 3 backplane if the Zone 3 K2 keying feature is removed.

ATCA® 3.0 Modules may have a Zone 3 connector or may have extensions in the Zone 3 area that may interfere with the AXIe 3.1 Zone 3 backplane.

ATCA® 3.0 Modules may have component interference with the guide pin or the AXIe 3.1 Zone 3 backplane connector.

1.7.2 Electrical Architecture Overview

1.7.2.1 System and Instrument Slots

An AXIe 3.1 backplane has a system slot and up to 15 instrument slots. The system slot is always located in logical slot 1, while the instrument slots are located in logical slots 2 through 15 consistent with the ATCA® specification. The logical slot numbering of the Zone 3 backplane must be consistent with the physical numbering scheme used on the ATCA® or AXIe 1.0 chassis.

1.7.2.2 Backplane Identification

There is a serial I²C EEPROM installed on the Zone 3 backplane accessible from the IPMC in the System Module to provide FRU identification.

1.7.2.3 System Slot Overview

The System slot (logical slot 1) of the Zone 3 backplane provides the unique connection to all slots in the backplane and to the DUT. The System Module interface group comprises of bussed signals (for utility interfaces) and point-to-point signals to support triggering to each slot. The DUT Interface signal group provides the serial I²C bus interface, Power supplies for circuitry typically found on DUT Load boards, a DUT Analog Bus that may be connected to the Zone 3 Analog Bus, and DUT I/O signals.

A typical n slot signal interconnect diagram is shown in Figure 1-1 illustrating signal groups and DUT I/O on the System Slot.
1.7.2.4 Instrument Slot Overview

In the Zone 3 backplane, there are 2 groups of signals in each Instrument slot (logical slots 2 through 16): the System Module Interface signal group and the DUT Interface signal group. The System Module interface group comprises of bussed signals (for utility interfaces) and point-to-point signals to support triggering. The DUT Interface signal group provides the serial I²C bus interface and DUT I/O signals. There are 152 DUT I/O signals available in the Instrument slot.

Figure 1-2 below illustrates the signal group available from the Instrument slots and those signals available at the DUT.
1.7.2.5 Zone 3 Backplane Connectors

Various types of the standard VHDM family connectors are used in the Zone 3 backplane, and installed in a mid-plane fashion. Depending upon the number of Instrument slots in the backplane, the System slot connector may comprise of multiple connectors to provide the required point-to-point connections for triggering resources.

1.7.2.6 Triggers and Synchronization

AXIe 3.1 provides triggering and synchronization resources beyond those of AXIe 1.0:

- Four (4) differential star-distributed trigger signal pairs (DSTARA through DSTARD) between each Instrument slot and the System slot. Each is a bi-directional differential terminated LVDS signal pair. All of the DSTAR pairs are all of matched length. Typical uses include triggering multiple modules independently with low skew, monitoring a trigger event from Instrument slots, and routing triggers between Instrument slots. Also, the low slot-to-slot skew and signal-to-signal skew make it possible to transfer a clock and synchronous trigger.
- Five (5) differential star-distributed user-synchronization signal pairs (USER_SYNC0 through USER_SYNC4) between each Instrument Module and the System Module, for system-defined instrument synchronization protocols. Potential uses include tight synchronization between Instrument Modules in a chassis, providing matched length custom clocking, or providing specialized or tightly timed synchronous triggers.

Figure 1-3 below is a block diagram of the AXIe 3.1 triggering and synchronization additions to AXIe 1.0.
1.7.2.7 Interoperability with AXIe 1.0 and ATCA® PCMIG® 3.0
AXIe 3.1 is based upon the AXIe 1.0, ATCA® PCMIG® 3.0 and ATCA® PCMIG® 3.4 specifications using PCIe signaling on the Zone 2 data fabric.

Test extensions added in AXIe 3.1 require additional System Module functionality as specified in the AXIe 1.0 and ATCA® PCMIG® 3.0 specifications. The additional features of the System Module include signal support found in the Zone 3 connector. These additional features supported in the System Module are:

1. Calibration Bus
2. Analog Bus
3. DUT Analog Bus
4. DSTAR point-to-point Instrument Module triggering
5. USER Sync Instrument Module support
6. Control signal support
7. FRU ID support

AXIe 1.0 System Modules may not include the additional features listed and may prevent Instrument Module operation.

AXIe 1.0 Instrument Modules can be installed in AXIe 3.1 compatible chassis with restrictions or limitation identified in the AXIe 1.0 specification.

1.8 Conformance Requirements
All AXIe 3.1 products including backplanes, subracks, chassis, and modules, are required to conform to the requirements of this specification.

1.9 References
- AXIe 1.0: Base Architecture Specification, AXIe Consortium.
2. Mechanical Requirements

This section defines the mechanical requirements for AXIe 3.1 backplane interface. It discusses the number of slots, the location of the System slot, chassis requirements, connector requirements, module types, and the interoperability of the System Module with the backplane.

2.1 Drawing Standard

The drawings in this specification shall be interpreted per ANSI Y14.100.

2.2 Dimensional Units

Dimensions in this specification are in millimeters unless otherwise specified.

2.3 Zone 3 Backplane Interface

2.3.1 Minimum Number of Slots

RULE 2-1: An AXIe 3.1 backplane SHALL at least have one AXIe 3.1 System slot and one Instrument slot.

2.3.2 Maximum Number of Slots

The maximum number of slots is limited by the size of the ATCA® or AXIe 1.0 chassis that includes the AXIe 3.1 backplane. ATCA® chassis may have a maximum of 16 slots, while AXIe 1.0 chassis have a maximum of 14 slots. The electrical definition of the AXIe 3.1 backplane is specified to support a maximum of 16 slots.

RULE 2-2: An AXIe 3.1 backplane SHALL NOT have more than 16 slots.

2.3.3 Slot Location

The intent of the AXIe 3.1 specification is that the AXIe 3.1 System Module is also the ATCA hub 1 module or the AXIe 1.0 System Module. Thus the AXIe 3.1 backplane’s system slot must also be logical slot 1. All other slots are instrument slots.

RULE 2-3: The System slot SHALL be defined as the Hub 1 slot in an ATCA® Chassis/backplane. This is the first logical slot but may be some other physical slot.

RULE 2-4: Instrument slots SHALL be defined beginning at logical slot 2 and may utilize up to a maximum of 15 slots to logical slot 16.

2.3.4 Slot Numbering

AXIe 3.1 backplane slot numbering is handled the same way the AXIe 1.0 and the ATCA® 3.0 Specifications and require:

RULE 2-5: AXIe 3.1 backplane with a System slot SHALL meet the slot numbering requirements set in the AXIe 1.0 and the ATCA® 3.0 Specifications for Hub logical 1 slot.

RULE 2-6: AXIe 3.1 backplane Instrument slots SHALL meet the slot numbering requirements set in the AXIe 1.0 and the ATCA® 3.0 Specification for Module/Node slots.

PERMISSION 2-1: Slot orientation and numbering schemes other than those defined in ATCA® MAY be used as long as it is clear and logical for the end user.

2.3.5 Backplane Dimensions

Since an AXIe 3.1 Zone 3 backplane can be installed in an ATCA® or AXIe 1.0 chassis, the following rules apply.

RULE 2-7: The AXIe 3.1 Zone 3 backplane SHALL meet the size, mechanical mounting hole, and tolerance requirements as defined for Zone 3 midplanes in the ATCA® 3.0 specification.
2.3.6 Zone 3 Backplane Connector Requirements
The Zone 3 backplane utilizes the VHDM connector series from Molex and Amphenol-TCS. Each Instrument slot utilizes a right guide, shield end, 8-row, 25-column, VHDM connector, for DUT I/O and test system extensions. The System Slot also utilizes the same connector and 2 additional open end, 8-row, 10-column, unguided connectors supporting the point-to-point signals required for the test extensions.

Table 2-1 identifies the backplane connectors required for System and Instrument Module slot locations. Equivalent connectors may also be utilized.

<table>
<thead>
<tr>
<th>Item</th>
<th>Molex Part Number</th>
<th>Amphenol-TCS Part Number</th>
<th>Description</th>
<th>Qty</th>
<th>Usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>74062-2501</td>
<td>495-5025-001</td>
<td>Guide Right, Shield-End, 8-Row, 25-column Straight Header with 200 signals.</td>
<td>1</td>
<td>All Zone 3 slots.</td>
</tr>
<tr>
<td>2</td>
<td>74060-1001</td>
<td>493-5010-001</td>
<td>Open-End, 8-row, 10-column, Straight Header with 80 signals.</td>
<td>2</td>
<td>Additional Zone 3 System slot connectors</td>
</tr>
</tbody>
</table>

Table 2-1: Zone 3 Backplane Connectors (Front Side)

2.3.6.1 Backplane Connector Locations
The Zone 3 connector locations are shown in Figure 2-1 below. The figure represents a typical 14 slot backplane configuration showing the System Module in slot 7 and Instrument Modules in all other slot locations.
Drawing Notes:
1. See Item 1 in Table 2-1.
2. See Item 2 in Table 2-1.
3. Backplane thickness is not specified in AXIe 3.1.

Figure 2-1: Typical Zone 3 Backplane Drawing illustrating Connector Locations
2.3.6.2 Mechanical Alignment and Keying
AXIe 3.1 modules utilize the A1/K1 alignment and keying feature associated with the Zone 2 connector as specified in the AXIe 1.0 and ATCA® 3.0 specifications.

AXIe 3.1 compatible Modules do not make use of the A2/K2 alignment and keying feature as specified in the AXIe 1.0 and ATCA® 3.0 specifications. When AXIe 1.0 Modules or ATCA® front boards are installed in a chassis with an AXIe 3.1 compatible Zone 3 backplane, they must have the K2 alignment feature removed before installation into the chassis.

2.3.6.3 System Slot
RULE 2-8: The AXIe 3.1 System slot location SHALL be the same as Logical slot 1 location of AXIe 1.0 and ATCA® 3.0 specifications.
RULE 2-9: The AXIe 3.1 System slot location SHALL NOT include the A2 keying feature specified in the ATCA® 3.0 specification.
RULE 2-10: The AXIe 3.1 System slot SHALL include the VHDM connectors illustrated in Figure 2-3 identified by Notes 1 and 2.

2.3.6.4 Instrument Slots
RULE 2-11: AXIe 3.1 Instrument slot location SHALL be the same as AXIe 1.0 and ATCA® 3.0 specification for Logical/Physical slots 2 through 16.
RULE 2-12: The AXIe 3.1 Instrument slot location SHALL NOT include the A2 keying feature specified in the ATCA® 3.0 specification.
RULE 2-13: The AXIe 3.1 Instrument slot SHALL include the VHDM connector illustrated in Figure 2-3 identified by Note 1.

2.4 System Module Requirements
RULE 2-14: The AXIe 3.1 System Module SHALL conform to the Front Board mechanical specifications identified in ATCA® 3.0.
RULE 2-15: The AXIe 3.1 System Module SHALL NOT include the K2 keying feature specified in the ATCA® 3.0 specification.
RULE 2-16: The AXIe 3.1 System Module SHALL NOT include the optional Zone 3 extension specified in the ATCA® 3.0 specification.
RULE 2-17: The AXIe 3.1 System Module SHALL include a Zone 3 VHDM connector illustrated in Figure 2-2.
2.5 Instrument Module Requirements

RULE 2-18: The AXIe 3.1 Instrument Module SHALL conform to the Front Board mechanical specifications identified in ATCA® 3.0.

RULE 2-19: The AXIe 3.1 Instrument Module SHALL NOT include the K2 keying feature specified in the ATCA® 3.0 specification.
RULE 2-20: The AXIe 3.1 Instrument Module SHALL incorporate a Zone 3 connector illustrated in Figure 2-3.

RULE 2-21: The AXIe 3.1 Instrument Module SHALL NOT include the optional Zone 3 extension specified in the ATCA® 3.0 specification.

PERMISSION 2-2: AXIe 1.0 Instrument Modules MAY be installed in an AXIe 3.1 backplane.

PERMISSION 2-3: ATCA® Modules MAY be installed in an AXIe 3.1 backplane if the K2 keying feature is removed and there is no Zone 3 connector or Zone 3 area extension.

Drawing Notes:
1. ATCA® K2 keying feature must not be installed.
2. Use Molex part number 74040-1343.
3. All dimensions are referenced from datum D and E.

Figure 2-3: Instrument Module VHDM Zone 3 Connector Location
2.6 Zone 3 Rear Transition Module Usage

Zone 3 rear transition modules are not required or specified in the AXIe 3.1 specification. AXIe 3.1 completely specifies the Instrument and System Module connectors on the front side of the Zone 3 backplane, but many alternatives are possible for routing signals from the System and Instrument Modules to the rear of the Zone 3 backplane. Some alternatives are listed below:

1. Pass thru signals on Zone 3 from the front side to the back side using the appropriate rear side VHDM connectors.

2. VHDM cable assemblies connected directly to the rear side of the Zone 3 backplane

3. RTM's may be used as an interface from the rear side of Zone 3 to application specific cable assemblies.

4. Many other configurations possibilities.
3. Electrical Requirements

3.1 Control Signals

3.1.1 Reset Signal Requirements

The RESET signal is a differential M-LVDS bussed signal connecting all slots of the Zone 3 backplane. The reset signal is a positive true signal driven by the System Module. The signal typically originates from the test computer’s PCIe cable reset signal. Each System and Instrument Module should reset to their power-on state when the RESET signal is asserted.

3.1.1.1 Backplane Requirements

RULE 3-1: The backplane SHALL differentially terminate the RESET signal pair with a resistance of 40 \(\Omega\) to 110 \(\Omega\).

3.1.1.2 Module Requirements

RULE 3-2: The System Module SHALL drive the differential M-LVDS positive true RESET signal on the backplane upon receipt of a similar reset signal from the test computer.

RULE 3-3: The Instrument Module SHALL receive an LVDS RESET signal from the backplane.

RULE 3-4: The Modules SHALL limit the trace length to a maximum length of 38mm from the M-LVDS driver/receiver pins to the backplane connector pins.

RULE 3-5: The Modules SHALL route the RESET signal with a balanced transmission line pair having a differential impedance of 100 \(\Omega\) \(\pm\) 10 \(\Omega\) to the backplane.

RULE 3-6: The RESET signal pair SHALL be matched in length to less than 1.3 mm.

RULE 3-7: The Modules SHALL reset to their power-on state when the RESET signal is asserted.

OBSERVATION 3-1: The System Module receives a PCIe cable reset signal from the test computer and uses this signal as the source to drive the reset signal as specified in RULE 3-2.

3.1.2 DUT Power On Signal Requirements

The DUT_PWR_ON signal is used to enable or disable power and signals driven by Modules to the DUT I/O connector pins of the Zone 3 backplane. Application load boards or test fixtures may be changed at any time DUT testing is not in progress. To facilitate the inserting or removal of these test fixtures, it is good practice to remove power and disable signals to the DUT I/O by de-asserting the DUT_PWR_ON signal prior to changing test fixtures. Once installed, DUT_PWR_ON must be applied prior to instrument module software execution.

The DUT_PWR_ON signal is driven by the System Module indicating that DUT power is enabled and available at the DUT I/O connector of the System Module. When the DUT_PWR_ON signal is active, Instrument Modules may connect their DUT I/O, Calibration Bus, Analog Bus and DUT Analog Bus signals on the Zone 3 backplane. When the DUT_PWR_ON signal is in-active, the Modules must disconnect their DUT I/O and the connections to the Calibration Bus, the Analog Bus and the DUT Analog Bus from the Zone 3 backplane connector. Refer to Section 3.2 and Section 3.5.

The DUT_PWR_ON signal is a differential M-LVDS bussed signal connecting all slots of the Zone 3 backplane.

3.1.2.1 Backplane Requirements

RULE 3-8: The backplane SHALL differentially terminate the DUT_PWR_ON signal pair with a resistance of 40 \(\Omega\) to 110 \(\Omega\).

3.1.2.2 Module Requirements

RULE 3-9: The System Module SHALL drive an M-LVDS DUT_PWR_ON signal on the backplane.

RULE 3-10: The Instrument Module SHALL receive an LVDS DUT_PWR_ON signal from the backplane.
RULE 3-11: The Module’s SHALL limit the trace length of the DUT_PWR_ON signal to a maximum length of 38mm from the M-LVDS driver pins to the backplane connector pins.

RULE 3-12: The Module’s SHALL route the DUT_PWR_ON signal with a balanced transmission line pair having a differential impedance of 100 Ω ± 10 Ω to the backplane.

RULE 3-13: The DUT_PWR_ON signal pair SHALL be matched to less than 1.3mm.

3.1.3 Reserved Signal Requirements

There are 4 pairs of differential signals designed to support M-LVDS signals. Each pair has the characteristic impedance of 130Ω and differentially terminated at both ends with 80.6 Ω resistors installed on the Zone 3 backplane. The reserved signals are routed in the Zone 3 backplane and are reserved for future use.

3.1.3.1 Backplane Requirements

RULE 3-14: The backplane SHALL route the 4 RESERVED signals with balanced transmission line pairs having a differential impedance of 130 Ω ± 10 Ω bussed to all slots in the backplane.

RULE 3-15: The backplane SHALL differentially terminate each of the 4 RESERVED differential signal pairs with 80.6 Ω resistors at each end of the backplane.

3.1.3.2 Module Requirements

PERMISSION 3-1: The Modules MAY connect to the RESERVED signals using M-LVDS transceivers.

RULE 3-16: The Module’s SHALL limit the trace length to a maximum length of 38mm from the Module’s M-LVDS transceiver pins to the backplane connector pins.
3.2 Analog and Calibration Bus Signals

The AXIe 3.1 specification includes a 4 wire calibration bus (CBUS set) and a 2 lane 2 wire analog bus (ABUS set) in the AXIe 3.1 backplane. The 4 wire calibration bus includes high force & sense and low force & sense signals on the backplane. The analog bus includes 2 channels, each with a force & sense connection to the backplane. The analog bus may be extended to the DUT via the System slot as illustrated in Figure 3-1. This figure shows a typical interconnection between the buses usually implemented on the System Module.

![Figure 3-1: Typical Calibration and Analog Bus Connect Relays on System Module](Image)

**RULE 3-17:** An ABUS set SHALL be defined as containing the 2 ABUS signal pairs (ABUS_1_FORCE & ABUS_1SENSE and ABUS_2_FORCE & ABUS_2SENSE).

**RULE 3-18:** A DUT_ABUS set shall be defined as containing the 2 DUT ABUS signal pairs (DUT_ABUS_1_FORCE & DUT_ABUS_1SENSE and DUT_ABUS_2_FORCE & DUT_ABUS_2SENSE).

**RULE 3-19:** A CBUS set SHALL be defined as containing the 2 CBUS signal pairs (CAL_HI_FORCE & CAL_HISENSE and CAL_LO_FORCE & CAL_LOSENSE).

**RULE 3-20:** The Module’s ABUS set, DUT_ABUS set and CBUS set SHALL include disconnect switches isolating the internal modules circuitry from the backplane capable of withstanding up to 100Vdc.

**RULE 3-21:** The Module’s ABUS set, DUT_ABUS set and CBUS set SHALL be disconnected from the backplane if the DUT Power On signal (DUT_PWR_ON) is in-active.
OBSERVATION 3-2: The ABUS set, DUT_ABUS set and CBUS set disconnect switches isolating the Module from the backplane require both the assertion of signal DUT_PWR_ON and software control to reconnect on the backplane.

3.2.1 Analog Bus Interface Requirements

The Analog Bus (ABUS set) includes 2 pair of signals supporting 2 independent busses, each with a force and sense connection bussed to all slots on the backplane. In addition to the Zone 3 Analog Bus, a DUT Analog Bus is also provided on the System Modules DUT I/O connector with isolation from the Analog Bus. The DUT and Analog Bus use is not specified in the AXIe 3.1 specification but may be used for DC or low frequency signal applications from one instrument module to one or many instrument modules.

3.2.1.1 Backplane Requirements

RULE 3-22: Each ABUS set pair SHALL be routed to all slots on the backplane as differential pairs.

RECOMMENDATION 3-1: The DUT_ABUS set SHOULD be connected on the Zone 3 backplane from the System slot.

3.2.1.2 System Module Requirements

RECOMMENDATION 3-2: The System Module SHOULD include a connection from the ABUS set to the DUT_ABUS set.

PERMISSION 3-2: The System Module MAY include a connection path from the ABUS set to an external instrument.

RULE 3-23: If the System Module connects the ABUS set to the DUT_ABUS set, the signals SHALL be connected to the System slot according to Table 3-1.

<table>
<thead>
<tr>
<th>ABUS Set</th>
<th>DUT_ABUS Set</th>
</tr>
</thead>
<tbody>
<tr>
<td>ABUS_1_FORCE</td>
<td>DUT_ABUS_1_FORCE</td>
</tr>
<tr>
<td>ABUS_1SENSE</td>
<td>DUT_ABUS_1SENSE</td>
</tr>
<tr>
<td>ABUS_2_FORCE</td>
<td>DUT_ABUS_2_FORCE</td>
</tr>
<tr>
<td>ABUS_2SENSE</td>
<td>DUT_ABUS_2SENSE</td>
</tr>
</tbody>
</table>

Table 3-1: ABUS Set to DUT_ABUS Set Connection Path

3.2.1.3 Instrument Module Requirements

The Instrument Modules connection to the Analog Bus is optional and its use is instrument defined.

PERMISSION 3-3: The Instrument Module MAY connect to the ABUS 1 or both ABUS 1 and ABUS 2.

RULE 3-24: When an Instrument Module does not implement both Analog Buses, the implemented Analog Bus SHALL be ABUS 1.

3.2.2 Calibration Bus Interface Requirements

The AXIe 3.1 specification includes a 4 wire calibration bus on the Zone 3 backplane. The 4 wire calibration bus (CBUS set) includes a high force & sense signal and a low force & sense signal. The Calibration bus is typically used for DC calibration of Instrument Modules. A NIST traceable instrument is typically connected to the Calibration Bus on the System Module.
3.2.2.1 Backplane Requirements

RULE 3-25: Each CBUS set pair SHALL be routed to all slots on the backplane as differential pairs.

3.2.2.2 System Module Requirements

PERMISSION 3-4: The System Module MAY include a connection path from the CBUS set to an external instrument.

RECOMMENDATION 3-3: The System Module SHOULD include a connection to the CBUS set on the backplane.

RECOMMENDATION 3-4: The System Module SHOULD connect the CBUS set to the ABUS set through disconnect switches according to Table 3-2.

<table>
<thead>
<tr>
<th>CBUS Set</th>
<th>ABUS Set</th>
</tr>
</thead>
<tbody>
<tr>
<td>CBUS_HI_FORCE</td>
<td>ABUS_1_FORCE</td>
</tr>
<tr>
<td>CBUS_HI_SENSE</td>
<td>ABUS_1_SENSE</td>
</tr>
<tr>
<td>CBUS_LO_FORCE</td>
<td>ABUS_2_FORCE</td>
</tr>
<tr>
<td>CBUS_LO_SENSE</td>
<td>ABUS_2_SENSE</td>
</tr>
</tbody>
</table>

Table 3-2: CBUS Set to ABUS Set Connection Path

3.2.2.3 Instrument Module Requirements

The Instrument Modules connection to the Calibration Bus is optional and its use is instrument defined.

PERMISSION 3-5: The Instrument Module MAY connect to the Calibration Bus.

3.3 Star Trigger Signals

In addition to the AXIe 1.0 triggers, the AXIe 3.1 specification has included four independent triggers for each Instrument slot. The DSTARA, DSTARB, DSTARC, and DSTARD signals are differential point-to-point connections between the System slot and the Instrument slots. For each of these four signals, there is an independent differential pair between each Instrument slot and the System slot. Additionally, all signals are matched length, and allow for transmission in either direction (i.e. System Module to Instrument Module or vice versa).

DSTAR<A..D> are designed for sending high-speed, high-quality trigger or clock signals between the System Module and the Instrument Modules. AXIe 3.1 does not specify the full functionality of the triggering subsystem of the System Module.

3.3.1 Backplane Requirements

There will be a set of four differential pairs connecting each Instrument slot to the System slot in a star configuration for the purpose of timing and synchronization. These differential pairs will be referred to as a DSTAR set (as defined below).

RULE 3-26: A DSTAR set SHALL be defined as containing the four differential signal pairs (DSTARA\text{n}, DSTARB\text{n}, DSTARC\text{n}, and DSTARD\text{n}), where \text{n} denotes the logical slot number for each Instrument slot.

RULE 3-27: All differential pairs within a DSTAR set SHALL be routed to the same logical slot.

RULE 3-28: If a DSTAR set is routed to a Instrument slot, its signals SHALL be connected to the Instrument slot according to Table 3-3, where \text{n} denotes the logical slot number.
### Table 3-3: DSTAR<A..D> Logical Slot Mapping

<table>
<thead>
<tr>
<th>Differential Star Pair from System Slot</th>
<th>Instrument Slot Pair</th>
</tr>
</thead>
<tbody>
<tr>
<td>DSTARAn+</td>
<td>DSTARA+</td>
</tr>
<tr>
<td>DSTARAn-</td>
<td>DSTARA-</td>
</tr>
<tr>
<td>DSTARBn+</td>
<td>DSTARB+</td>
</tr>
<tr>
<td>DSTARBn-</td>
<td>DSTARB-</td>
</tr>
<tr>
<td>DSTARCn+</td>
<td>DSTARC+</td>
</tr>
<tr>
<td>DSTARCn-</td>
<td>DSTARC-</td>
</tr>
<tr>
<td>DSTARDn+</td>
<td>DSTARD+</td>
</tr>
<tr>
<td>DSTARDn-</td>
<td>DSTARD-</td>
</tr>
</tbody>
</table>

**RULE 3-29:** Every Instrument slot SHALL have a DSTAR set routed to it from the System slot.

**OBSERVATION 3-3:** The pinout for the System slot was chosen so that when placed in the middle of a backplane, the signal lengths can be kept to a minimum and the layer count will be minimized by keeping all or most of the differential pairs on one routing layer.

**RULE 3-30:** The backplane SHALL route the DSTAR signals to each slot with balanced transmission line pairs having a differential impedance of $100 \Omega \pm 10 \Omega$.

**PERMISSION3-6:** Each DSTARA, DSTARB, DSTARC, and DSTARD pairs SHOULD be routed on a single layer referenced to a solid ground plane to improve radiated immunity when traces are floating.

**RULE 3-31:** The DSTAR pairs (including all DSTARA, DSTARB, DSTARC, and DSTARD signals) across the backplane SHALL be matched to less than 1.3 mm.

**RULE 3-32:** Each DSTAR pair (including all DSTARA, DSTARB, DSTARC, and DSTARD pairs) across the backplane SHALL be matched to less than 1.3 mm.

### 3.3.2 System Module Requirements

A System Module will connect to one or more signals of all DSTAR sets for all logical slots. All DSTAR signals allow bidirectional operation.

**RULE 3-33:** The System Module must implement at a minimum DSTARA for each Instrument Module. In addition, the System Module must implement a minimum trigger subsystem that allows any of the Instrument Module’s DSTARA signals to connect to any other Instrument Module’s DSTARA.

**PERMISSION3-7:** System Modules SHOULD implement all signals of a DSTAR set, including a trigger subsystem that allows robust connection of any Instrument Module DSTARs to any other Instrument Module’s DSTARs.

**RULE 3-34:** Each signal of each DSTAR set provided by the System Module SHALL be a differential M-LVDS signal. The System Module SHALL connect all signals of a DSTAR set to the backplane connector with a balanced transmission line pair having a differential impedance of $100 \Omega \pm 10 \Omega$.

**RULE 3-35:** Each signal of each DSTAR set provided by the System Module SHALL be terminated at the source with a $100 \Omega$ differential load.

**RULE 3-36:** When a DSTAR pair is terminated with a $100 \Omega$ differential load at the Receiver, and the driver is enabled, the voltage levels at the connector to the System Module SHALL be compliant with the TIA/EIA-899 M-LVDS specification.
RULE 3-37: The signal source SHALL ensure that the LVDS transceiver is off by default, and SHALL only enable it under software control when a Receiver with a 100 Ω differential termination resistor is known to exist.

RULE 3-38: Each DSTARA, DSTARB, DSTARC, and DSTARD signal to each Instrument slot SHALL be driven by an independent differential LVDS transceiver.

PERMISSION3-8: System Modules SHOULD specify the maximum skew between all DSTARA, DSTARB, DSTARC, and DSTARD signals, as provided to the pins of the connectors on the System Module which connect it to the backplane.

PERMISSION3-9: System Modules SHOULD specify the maximum delay for all DSTARA, DSTARB, DSTARC, and DSTARD signals, between the pins of the connectors on the System Module which connect it to the backplane and the trigger subsystem.

3.3.3 Instrument Module Requirements

An Instrument slot will connect to a unique DSTAR set from the System slot. All DSTAR signals allow bidirectional operation.

RULE 3-39: Each signal of the DSTAR set provided by the Instrument Module SHALL be a differential M-LVDS signal. The Instrument Module SHALL transmit each signal to the backplane connector with a balanced transmission line pair having a differential impedance of 100 Ω ± 10 Ω.

RULE 3-40: Each signal of each DSTAR set provided by the Instrument Module SHALL be terminated at the source with a 100 Ω differential load.

RULE 3-41: When a DSTAR pair is terminated with a 100 Ω differential load at the Receiver, and the driver is enabled, the voltage levels at the connector to the Instrument Module SHALL be compliant with the TIA/EIA-899 M-LVDS specification.

RULE 3-42: The signal source SHALL ensure that the M-LVDS transceiver is off by default, and SHALL only enable it under software control when a Receiver with a 100 Ω differential termination resistor is known to exist.

RULE 3-43: Each DSTARA, DSTARB, DSTARC, and DSTARD signal to each System slot SHALL be driven by an independent differential LVDS transceiver.

PERMISSION3-10: Instrument Modules SHOULD specify the maximum skew between all DSTARA, DSTARB, DSTARC, and DSTARD signals, as provided to the pins of the connectors on the Instrument Module which connect it to the backplane.

PERMISSION3-11: Instrument Modules SHOULD specify the maximum delay for all DSTARA, DSTARB, DSTARC, and DSTARD signals, between the pins of the connectors on the Instrument Module which connect it to the backplane and the trigger subsystem.

PERMISSION 3-12: Instrument Modules MAY implement 0, 1, 2, 3, or all signals of a DSTAR set.

RULE 3-44: In the case when an Instrument Module does not implement all four signals of a DSTAR set, the implemented DSTAR signals should start with DSTARA for the first implemented signal, and proceed in order through DSTARD for the fourth implemented signal.

3.4 Star User Signals

AXIe 3.1 provides five differential point-to-point connections between the System slot and the Instrument slots to be used for user-defined synchronization. For each of these five signals, there is an independent differential pair between each Instrument slot and the System slot. Additionally, all signals are matched length, and allow for transmission in either direction (i.e. System Module to Instrument Module or vice versa).

USER_SYNC<0..4> are designed for sending high-speed, high-quality synchronization signals between the System Module and the Instrument Modules. AXIe 3.1 does not specify the functionality of the user-defined synchronization subsystem of the System or Instrument Modules or even require that the system be constructed with a user-defined synchronization subsystem.
3.4.1 Backplane Requirements

There will be a set of five differential pairs connecting each Instrument slot to the System slot in a star configuration for the purpose of timing and synchronization. These differential pairs will be referred to as a USER_SYNC set (as defined below).

**RULE 3-45:** A USER_SYNC set SHALL be defined as containing the five differential signal pairs (USER_SYNC0n thru USER_SYNC4n), where n denotes the logical slot number for each Instrument slot.

**RULE 3-46:** All differential pairs within a USER_SYNC set SHALL be routed to the same logical slot.

**RULE 3-47:** If a USER_SYNC set is routed to an Instrument slot, its signals SHALL be connected to the Instrument slot according to Table 3-4, where n denotes the logical slot number.

<table>
<thead>
<tr>
<th>User Sync Pair from System Slot</th>
<th>Instrument Slot Pair</th>
</tr>
</thead>
<tbody>
<tr>
<td>USER_SYNC0n+ USER_SYNC0n-</td>
<td>USER_SYNC0+ USER_SYNC0-</td>
</tr>
<tr>
<td>USER_SYNC1n+ USERSYNC1n-</td>
<td>USER_SYNC1+ USER_SYNC1-</td>
</tr>
<tr>
<td>USER_SYNC2n+ USER_SYNC2n-</td>
<td>USER_SYNC2+ USER_SYNC2-</td>
</tr>
<tr>
<td>USER_SYNC3n+ USER_SYNC3n-</td>
<td>USER_SYNC3+ USER_SYNC3-</td>
</tr>
<tr>
<td>USER_SYNC4n+ USER_SYNC4n-</td>
<td>USER_SYNC4+ USER_SYNC4-</td>
</tr>
</tbody>
</table>

**Table 3-4: USER_SYNC<0..4> Logical Slot Mapping**

**RULE 3-48:** Every Instrument slot SHALL have a USER_SYNC set routed to it from the System slot.

**OBSERVATION 3-4:** The pinout for the System slot was chosen so that when placed in the middle of a backplane, the signal lengths can be kept to a minimum and the layer count will be minimized by keeping all or most of the differential pairs on one routing layer.

**RULE 3-49:** The backplane SHALL route the USER_SYNC signals to each slot with balanced transmission line pairs having a differential impedance of $100 \pm 10 \Omega$.

**PERMISSION3-13:** All USER_SYNC0 through USER_SYNC4 pairs SHOULD be routed on a single layer referenced to a solid ground plane to improve radiated immunity when traces are floating.

**RULE 3-50:** The USER_SYNC pairs (including all USER_SYNC0 through USER_SYNC4 signals) across the backplane SHALL be matched to less than 1.3 mm.

**RULE 3-51:** Each USER_SYNC pair (including all USER_SYNC0 through USER_SYNC4 pairs) across the backplane SHALL be matched to less than 1.3 mm.

3.4.2 System Module Requirements

A System slot may connect to any or all USER_SYNC sets for all logical slots. All USER_SYNC signals allow bidirectional operation. There are no requirements on a System Module for the USER_SYNC functionality.

**PERMISSION3-14:** If a System Module implements a USER_SYNC subsystem, it SHOULD provide for an output disable for each USER_SYNC signal to allow mixing of Instrument Modules that use different USER_SYNC synchronization subsystems.
PERMISSION3-15: If a System Module implements a USER_SYNC synchronization subsystem, it SHOULD specify how it uses each USER_SYNC signal, whether it uses single-ended or differential signaling, the signal levels, and the timing characteristics. This is necessary for integrating System and Instrument Modules properly in an AXIe 3.1 chassis.

OBSERVATION 3-5: As there are no requirements placed on a User Synchronization subsystem, which by definition is intended for very specific synchronization of multiple instruments in a system, it is quite likely that System Modules developed with a specific User Synchronization subsystem will only work with specific Instrument Modules.

3.4.3 Instrument Module Requirements
An Instrument slot may connect to a unique USER_SYNC set from the System slot. All USER_SYNC signals allow bidirectional operation. There are no requirements on an Instrument Module for the USER_SYNC functionality.

PERMISSION3-16: If an Instrument Module implements a USER_SYNC subsystem, it SHOULD provide for an output disable for each USER_SYNC signal to allow mixing of Instrument Modules that use different USER_SYNC synchronization subsystems.

PERMISSION3-17: If an Instrument Module implements a USER_SYNC synchronization subsystem, it SHOULD specify how it uses each USER_SYNC signal, whether it uses single-ended or differential signaling, the signal levels, and the timing characteristics. This is necessary for integrating System and Instrument Modules properly in an AXIe 3.1 chassis.

3.5 DUT Signals

3.5.1 DUT I/O Interface Signal Requirements
The System Module supports up to 36 DUT I/O signals and each Instrument Module supports up to 152 DUT I/O signals on the Zone 3 backplane.

All Instrument Modules receive the DUT_PWR_ON signal from the backplane and must enable their DUT I/O signals, conversely, when the DUT_PWR_ON signal is in-active, the DUT I/O signals on all Modules are disconnected.

RULE 3-52: A System Slot DUT IO set SHALL be defined as containing the thirty six signals (DUTIO_CH1 thru DUTIO_CH36).

RULE 3-53: An Instrument Slot DUT IO set SHALL be defined as containing the one hundred and fifty two signals (DUTIO_CH1 thru DUTIO_CH152).

RULE 3-54: The Modules SHALL enable all signals in their DUTIO set via backplane signal DUT_PWR_ON.

RULE 3-55: The Module’s DUT I/O set SHALL be disconnected from the backplane if the DUT Power On signal (DUT_PWR_ON) is in-active.

PERMISSION 3-18: The Module’s DUT I/O MAY be disconnected from the backplane by driving 0V, tri-stated, or disconnected via a switch.

OBSERVATION 3-6: The DUT I/O set disconnect switches require both the assertion of signal DUT_PWR_ON and software control to re-connect on the backplane.

3.5.1.1 Backplane Requirements

RULE 3-56: The System Slot DUT IO set SHALL be connected on the System Slot Zone 3 backplane connector.

RULE 3-57: The Instrument Slot DUT IO set SHALL be connected on the Instrument Slots of the Zone 3 backplane connector.

3.5.1.2 Module Requirements

PERMISSION 3-19: The System Module MAY implement 0 or any number of signals in the System Slot DUTIO set.
3.5.2 DUT Power Supply Requirements

The System slot has provisions for supplying the DUT Load Board with up to 5 power supply voltage levels via the Zone 3 Backplane. The System Module may provide these voltages for powering applications circuitry typically found on load boards. These power supplies are enabled or disabled via the System Module typically controlled via software, but may be controlled by other means. When the System Module enables the DUT Power Supplies, the signal DUT_PWR_ON is active and driven by the System Module on the Zone 3 Backplane.

3.5.2.1 Backplane Requirements

RULE 3-58: A DUT Voltage set SHALL be defined as containing the five voltage levels (DUT_PWR_1, DUT_PWR_2, DUT_PWR_3, DUT_PWR_4 and DUT_PWR_5).

RULE 3-59: The backplane SHALL connect the DUT Voltage set from the System Slot to the backplane.

3.5.2.2 System Module Requirements

PERMISSION 3-21: The System Module MAY implement 0, 1, 2, 3, 4 or 5 voltage levels in the DUT Voltage set.

RULE 3-60: The System Module SHALL enable all voltages in the DUT Voltage set via signal DUT_PWR_ON on the backplane.

RULE 3-61: The System Module SHALL disable all voltages in the DUT Voltage set when signal DUT_PWR_ON is in-active on the backplane.

3.5.3 IPMI I²C FRU Identification Requirements

Each module has an FRU ID Interface. This interface allows an I²C master in the module to read ID EEPROMs on the Module, backplane, RTM, and other devices that may be attached to the RTM. Typically the module’s I²C bus originates from the module’s IPM controller and is connected to the FRU ID interface. Certain I²C device addresses are reserved for specific types of devices connected to the FRU ID interface, as shown in Table 3-5.

The FRU ID EEPROM data storage follows the Board Info Area Format of the IMPI Platform Management FRU Information specification.

<table>
<thead>
<tr>
<th>FRU ID</th>
<th>I²C 7 Bit Address Allocation</th>
<th>FRU ID EEPROM address assigned for:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Zone 3 Backplane</td>
<td>Address Range 0x50 – 0x57</td>
<td>Zone 3 backplane.</td>
</tr>
<tr>
<td>System Module or Instrument Module</td>
<td>0x51</td>
<td>System Module or Instrument Module.</td>
</tr>
<tr>
<td>RTM</td>
<td>0x52</td>
<td>RTM, if used.</td>
</tr>
<tr>
<td>Reserved</td>
<td>0x53</td>
<td>Reserved.</td>
</tr>
<tr>
<td>Reserved</td>
<td>0x54</td>
<td>Reserved.</td>
</tr>
<tr>
<td>Mezzanine Module #1</td>
<td>0x55</td>
<td>Optional Mezzanine Module #1 installed on the System or Instrument Module.</td>
</tr>
<tr>
<td>Mezzanine Module #2</td>
<td>0x56</td>
<td>Optional Mezzanine Module #2 installed on the System or Instrument Module.</td>
</tr>
<tr>
<td>Mezzanine Module #3</td>
<td>0x57</td>
<td>Optional Mezzanine Module #3 installed on the System or Instrument Module.</td>
</tr>
</tbody>
</table>

Table 3-5: FRU ID EEPROM Address Table

3.5.3.1 Backplane Requirements

RULE 3-62: An FRU ID Interface set SHALL be defined as containing the three I²C signals (FRU_ID_I2C_SDA, FRU_ID_I2C_SCK and FRU_ID_I2C+_5V).
RULE 3-63: The Zone 3 backplane SHALL have an FRU ID EEPROM addressed at I2C address 0x50 connected to the FRU ID Interface set of the System Slot.

RULE 3-64: The Zone 3 backplane SHALL connect the FRU ID Interface set from each Module slot to each backplane slot independently.

OBSERVATION 3-7: The System Slot and each Instrument Slot in the backplane has its own FRU ID Interface set. The backplane must keep each FRU ID Interface set independent and must not connect them together.

3.5.3.2 System Module and Instrument Module Requirements

RULE 3-65: The System Module and each Instrument Module SHALL provide an FRU ID Interface set to the backplane from their IPMC.

RULE 3-66: The System Module and each Instrument Module SHALL have an FRU ID EEPROM addressed at I2C address 0x51 and connected to their respective FRU ID Interface set.

RULE 3-67: If RTM’s are utilized on the System Slot or Instrument Slot they SHALL have an FRU ID EEPROM addressed at I2C address 0x52 and connected to their respective FRU ID Interface set.

RULE 3-68: If Mezzanine Modules are utilized on the System Module or Instrument Modules they SHALL have an FRU ID EEPROM addressed at I2C address 0x55, or 0x56, or 0x57 and connected to their respective FRU ID Interface set.

RULE 3-69: The System Module and each Instrument Module SHALL provide pull-up resistors on the FRU_ID_I2C_SDA and FRU_ID_I2C_SCK signals.

RULE 3-70: The System Module and each Instrument Module SHALL provide +5.0V ±10% for the FRU ID Interface set on signal FRU_ID_I2C_+5V.

RULE 3-71: The +5.0V power source for the FRU ID Interface set SHALL be available simultaneously with the power source used for the IMPC on each module.

OBSERVATION 3-8: The +5.0V power source for the FRU ID Interface set is provided directly from the -48VDC power source from the backplane allowing the IMPC of each module to identify FRU IDs in each FRU ID EEPROM without the need to apply power to the rest of the Module.

OBSERVATION 3-9: The I2C pull-up resistors as specified in RULE 3-69 should be selected based on the speed of the interface implemented by the Module.

3.5.4 I2C User Interface Requirements

The System Module and each Instrument Module may implement an I2C interface to the Zone 3 Backplane. The System Modules I2C User Interface may be used for application specific interfaces on the DUT Load Board or may be used on an RTM for general purpose control.

The Instrument Modules I2C User Interface may also be used on the RTM’s for general purpose control when populated with it’s own I2C devices.

Each I2C User Interface should contain an I2C transceiver, like the LTC4309, to protect the I2C interface in case RTM’s or DUT Load Boards are hot swapped.

3.5.4.1 Backplane Requirements

RULE 3-72: An I2C User Interface set SHALL be defined as containing the three I2C signals (USER_I2C_SDA, USER_I2C_SCK and USER_I2C_+5V).

RULE 3-73: The backplane SHALL connect the I2C User Interface set from each Module to each backplane slot independently.

OBSERVATION 3-10: The System Slot and each Instrument Slot in the backplane has its own I2C User Interface set. The backplane must keep each I2C User Interface set independent and must not connect them together.

3.5.4.2 System and Instrument Module Requirements

PERMISSION 3-22: Modules MAY implement the I2C User Interface set.
RULE 3-74: Modules SHALL provide pull-up resistors on the USER_I2C_SDA and USER_I2C_SCK signals.

RULE 3-75: Modules SHALL provide +5.0V ±10% for the \( I^2C \) User Interface on signal USER_I2C+_5V.
### 3.6 Zone 3 Backplane Connector Pin-Out and Signal Assignment

This section lists the connector pin-out and signal assignment of connectors used in the AXIe 3.1 compliant Zone 3 Backplane.

Signal naming convention:

1. The “LOGICAL_xx” in the signal name identifies the logical slot number of the signal name.
2. Differential signals are denoted by a trailing + (positive) or – (negative) symbol.

#### 3.6.1 System Slot Pin Assignments

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Table 3-6: Zone 3 (Front Side) System Slot Connector Signal Assignment

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### 3.6.2 Instrument Slot Pin Assignments

#### Instrument Slot Zone 3 Backplane Connector (Front Side)

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Table 3-7: Zone 3 (Front Side) Instrument Slot Connector Signal Assignment