AXIe 1.0 Specification Errata

Revision 1.0

April 28, 2011

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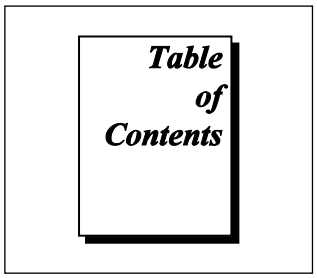

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AXIe 1.0 Specification Errata

Revision History

This section is an overview of the revision history of the AXIe 1.0 specification Errata.

Table 1-1. Errata Revisions

Revision Number	Date of Revision	Revision Notes
1.0	April 28, 2011	Initial version.

1. Introduction

The purpose of this errata document is to correct known errors and resolve ambiguities in the AXIe 1.0 Base Specification, Revision 1.0. This document addresses 3 classes of errata:

1. **Technical Errata:** These are errors in the document that have technical impact. In all cases, the errors are the result of editing mistakes that resulted in the document reflecting something different from the intent of the AXIe Technical Working Group. The corrections is this section supersede the corresponding content in the AXIe 1.0 Base Architecture Specification itself.
2. **Clarifications:** These are generally omissions or ambiguities that were not adequately resolved by the Technical Working Group prior to the publication of the specification. The entries in this section highlight these issues and reflect the current sense of the Technical Working Group regarding the resolution of these issues in future revisions of the AXIe Base Specification.
3. **Non-Technical Errata:** These are editorial mistakes such as typos, spelling errors, grammatical errors, and formatting errors that do not impact the technical content or interpretation of the specification. There are listed here for future reference by the Technical Working Group.

2. Technical Errata

2.1 Local Bus Pinout Table

Figure 6-1 (page 37) and Table 6-5 (page 43) incorrectly portray the AXIe Local bus pair numbers on connectors J20/P20 and J24/P24. Connector J20/P20 actually has local bus pairs 0-7 and 38-41. Connector J24/P24 actually has local bus pairs 18-37. The corrected Figure 6-1 is:

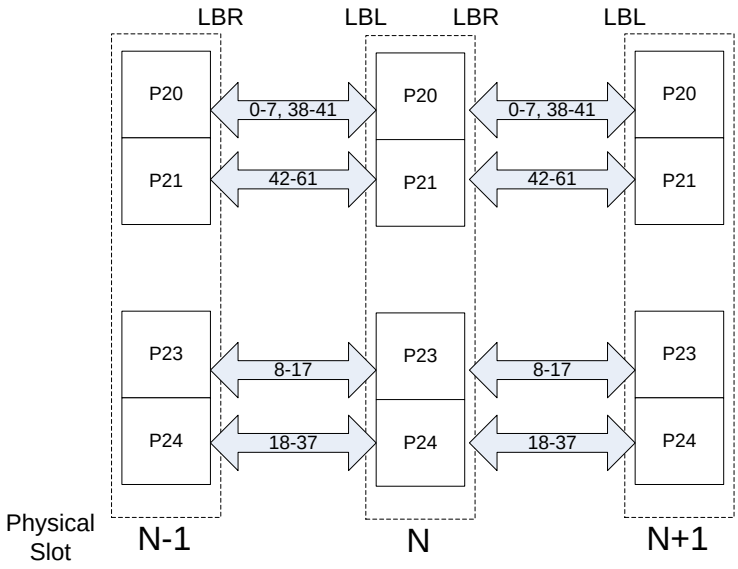

Figure 6-1: AXIe local bus backplane topology

The corrected Table 6-5 is:

Row	Interface	Instrument Slot (Logical Slot 2-14) J24/P24 Connector Pairs							
		ab		cd		ef		gh	
1	Local Bus	LBL[18]+	LBL[18]-	LBL[19]+	LBL[19]-	LBR[18]+	LBR[18]-	LBR[19]+	LBR[19]-
2	Local Bus	LBL[20]+	LBL[20]-	LBL[21]+	LBL[21]-	LBR[20]+	LBR[20]-	LBR[21]+	LBR[21]-
3	Local Bus	LBL[22]+	LBL[22]-	LBL[23]+	LBL[23]-	LBR[22]+	LBR[22]-	LBR[23]+	LBR[23]-
4	Local Bus	LBL[24]+	LBL[24]-	LBL[25]+	LBL[25]-	LBR[24]+	LBR[24]-	LBR[25]+	LBR[25]-
5	Local Bus	LBL[26]+	LBL[26]-	LBL[27]+	LBL[27]-	LBR[26]+	LBR[26]-	LBR[27]+	LBR[27]-
6	Local Bus	LBL[28]+	LBL[28]-	LBL[29]+	LBL[29]-	LBR[28]+	LBR[28]-	LBR[29]+	LBR[29]-
7	Local Bus	LBL[30]+	LBL[30]-	LBL[31]+	LBL[31]-	LBR[30]+	LBR[30]-	LBR[31]+	LBR[31]-
8	Local Bus	LBL[32]+	LBL[32]-	LBL[33]+	LBL[33]-	LBR[32]+	LBR[32]-	LBR[33]+	LBR[33]-
9	Local Bus	LBL[34]+	LBL[34]-	LBL[35]+	LBL[35]-	LBR[34]+	LBR[34]-	LBR[35]+	LBR[35]-
10	Local Bus	LBL[36]+	LBL[36]-	LBL[37]+	LBL[37]-	LBR[36]+	LBR[36]-	LBR[37]+	LBR[37]-

Table 6-1: J24/P24 Pin assignments for instrument slots (logical slots 2-14).

3. Clarifications

3.1 Local Bus Electrical Requirements

The electrical rules for the AXIe local bus in Section 6.9 (pages 52-53) are complicated by some practical constraints which include:

1. The IOs of current FPGA devices have a variety of input voltage limitations:
    a. For most configurable pins, the limit is the supply voltage + 0.5 V.
    b. Most configurable pins have diode clamps that are rated to sink a maximum of 10 mA.
    c. Dedicated gigabit SERDES pins have much lower maximum input voltages (i.e. 1.32 V).
2. There is potential for connections between AXIe local bus pins and AdvancedTCA® fabric or base interface pins.
3. AdvancedTCA® E-keying rules do not guarantee that incompatible IOs will always be prevented from applying signal voltages to the IO pins.
    a. Section 6.5.4 recommends, but does not require, that Base interface ports can be disabled by the E-keying mechanism.
    b. Section 6.6.2 recommends, but does not require, that Fabric interface ports can be disabled by the E-keying mechanism.
    c. AdvancedTCA® requires capacitor coupling at the receiver pins of fabric channel ports, and transformer coupling at all base channel ports.
    d. A disable fabric port's transmitters may be merely quiescent, In this state they may drive dc voltages onto the backplane, There are no common mode voltage constraints, The differential voltage is limited to a maximum of 1600 mV.
    e. Base interface port signal levels are defined by the relevant IEEE 802 specifications. The differential voltage may be as high as 2.5V.

AXIe Rules 6.77 and 6.78 currently require that Local Bus drivers and receivers that are at risk of connection to AdvancedTCA® fabric ports be tolerant of levels up to 3.6 V, and Local bus drivers and receivers that are at risk of connection to AdvancedTCA® base ports be tolerant of the base interface signal levels. These requirement are unrealistic, given the limitations mentioned in point #1 above.

We expect to replace Rules 6.77 and 6.78 with a number of observations and recommendations, including:

1. AXIe module designers need to be aware of the risks associated with a user inserting an AXIe module into an AdvancedTCA® shelf or inserting an AdvancedTCA® front board into an AXIe chassis. The likelihood of such events depends on the markets addressed by each module.
2. The highest risk scenario is the insertion of an AXIe module into an AdvancedTCA® hub slot. In this case, all of the local bus pairs 8-37 may be connected to active base interface ports, and all of the remaining local bus pairs to active fabric interface ports. The risk is similar if the module is inserted into an AXIe system slot.
3. A lower risk, but more likely, scenario is the insertion of an AXIe module into an AdvancedTCA® node slot. In most backplanes (dual-star topology), this may result in local bus pairs 8 and 9 connecting to an active base interface port. With a full-mesh topology backplane, there is the additional risk that local bus pairs 0-7 and 38-61 may be connected to active fabric ports.
4. Another scenario is the insertion of an AdvancedTCA® hub board into an AXIe instrument slot. This may result in the adjacent AXIe modules' local bus pairs being connected to active base ports (pairs 8-37) or active fabric ports (pairs 0-7 and 38-61).
5. The remaining scenario is the insertion of an AdvancedTCA® node board into an AXIe instrument slot. In most cases, this may result in the adjacent AXIe modules' local bus pairs 8 and 9 connecting to an active base interface port. If the AdvancedTCA® module is designed for full-mesh use there is the additional risk that the adjacent AXIe modules' local bus pairs 0-7 and 38-61 may be connected to active fabric ports.
6. To minimize the risk of damage from connection to active base interface ports, local bus pair 8-37 drivers and receivers should be 2.5V tolerant.

7. To minimize the risk of damage from connection to active fabric interface ports, local bus connections that require low-voltage drivers/receivers should use odd numbered local bus pairs within the ranges 1-7 and 39-61. These pairs correspond to AdvancedTCA® fabric port receive pairs that are capacitor coupled.
8. To minimize the risk of damage from connection to active fabric interface ports, even numbered local bus pairs in the ranges 0-6 and 38-60 should be tolerant of 1.6V differential and 2.5 V single-ended levels.

3.2 Trigger Bus Receivers

Section 6.8 of the AXIe Specification defines the requirements for the AXIe trigger bus. Currently the only driver/receiver electrical specification is shown in Figure 6-8, which shows MLVDS drivers and receivers. The document needs a Rule formalizing this requirement. In addition, we have a need for the Trigger Bus receivers to indicate a stable, valid state when the pair is not driven by any transmitter and the differential voltage is near zero. Thus we intend to include a requirement that AXIe Trigger bus receivers be Type 2 MLVDS. These receivers have a 100 mV input threshold offset and yield a deterministic stable output with a 0 V input.

4. Non-Technical Errata

4.1 AXIe Link Type Table Error

Table 3-8 (page 27), in its 7th entry, shows an incorrect range of reserved values. The correct range is 06h – Efh. The corrected table is:

Type	*Description*
00h	Reserved
01h	AXIe PCIe® Fabric Link
02h	AXIe FCLK
03h	AXIe CLK100
04h	AXIe SYNC
05h	AXIe STRIG
06h - EFh	Reserved
F0h - FEh	E-Keying OEM GUID Definition (per AdvancedTCA®)
FFh	Reserved

Table 3-1: AXIe Link Type.

4.2 Unnumbered Rule

On page 49, immediately before Figure 6-5, is an unnumbered RULE, "An AXIe 1.0 system module SHALL include the programmable capability for the SYNC output to operate either asynchronously or synchronously to CLK100**.**" This rule will become RULE 6.79:

RULE 6.79: An AXIe 1.0 system module SHALL include the programmable capability for the SYNC output to operate either asynchronously or synchronously to CLK100.