Accelerate Silicon Bring-up on the Bench

Semiconductor device complexity continues to grow with higher levels of integration coupled with smaller device geometries and increasing transistor counts. The validation and production test tasks are also made difficult by the increasing cost of testers that can provide all the functionality required properly validate the silicon. Techniques such as BIST (Built In Self Test) and SCAN are incorporated to increase fault coverage, but there is a disconnect between the fault coverage metrics, yield and final device quality.

As the devices grow in complexity the ATE patterns grow in both depth and number of pins required (i.e. multiple scan chains). ATE engineers have short time windows to release their test programs and struggle with having sufficient time on the production systems to complete their task.

Quality and Yield Enhancement engineers are also limited in tester time to run experiments and gather data to improve the process. With simpler devices engineering labs would utilize PXI and other low cost instruments to gather quality data. As parts have grown there is a need for ATE class instrumentation to be available within the lab environment with higher digital pin count, deep pattern memory and real ATE tools to debug the functional, SCAN and BIST patterns.

The instruments need to accept pattern formats from a variety of design and test tools. These pattern formats include industry standard STIL, WGL, SVF and custom formats. Pattern conversion as well as fail information processing is also required of test tools.

First Silicon

As part of chip manufacturing, the silicon is tested at both the wafer level and after packaging using automatic test equipment (ATE). This involves converting ATPG (i.e. SCAN and BIST) test patterns to a tester-specific format and generating a test program. When there are pattern fails, the ATE output is translated into chip failure data and processed by diagnosis tools.

Typically the SCAN and BIST data is sent back to the fab or test house customer for analysis as part of silicon bringup and quality/yield analysis. Going back and forth between a fab / test house and the customer is time consuming. Trying to get access to a tester with the silicon on it for further analysis and debug is generally difficult to practically impossible.

But what if you could eliminate the need for expensive tester equipment in the bring-up process, significantly reduce the cycle time, and achieve the same accuracy in diagnosis, using a bench setup and commercial software to run the ATPG patterns? You could expect a few key changes:

- lower silicon bring-up costs,
- significantly quicker diagnosis of the root cause of test pattern failures, and
- improved timeline to high quality and yield enhancement.

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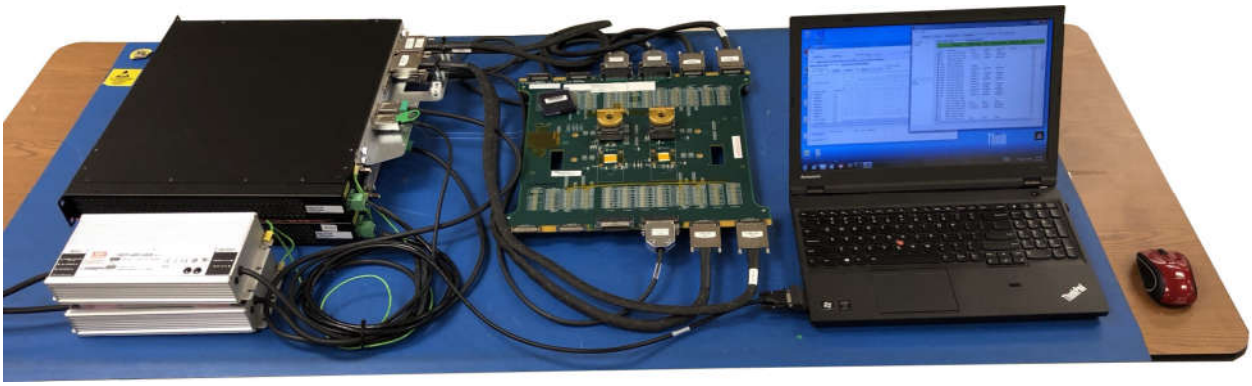
Test Evolution recently introduced the EV100 series of instruments based on modules used in the production ATE platform packaged in a 1U form factor with a cabled interface. Instruments are available for digital testing (192 channels per instrument) and DUT Power Supplies (48 channels per instrument).

The Test Evolution EV100 provides ATE class instrumentation packaged suitable for the lab or system test environment increasing the capability of characterization engineers to quickly execute device characterization suites in a bench top environment.

Customer Case Study

The EV100 has been used in customer labs interfaced to customer development cards via the VHDCI cable interface providing a low cost platform for pattern debug and device characterization without tying up expensive production ATE with up to 192 digital pins available for wide testing of multiple SCAN chains as well as interfacing to the JTAG port for device and customer development board setup. An example setup is shown the figure below.



A PC running commercial ATE software, along with a DUT validation board, cables, power supplies, and two EV100 ATE-class instruments fits nicely on a lab bench.

Typical validation systems can only run patterns at limited rates creating lengthy characterization shmoo times using tools such as the Mentor Tessent platform. An Opal Kelly compatible interface can be used to interface to existing characterization boards. The EV100-DD192 instrument can be connected thru this interface, and provide at speed testing with full timing and edge control allowing for device limited test speeds instead of limitations of some other test platforms.

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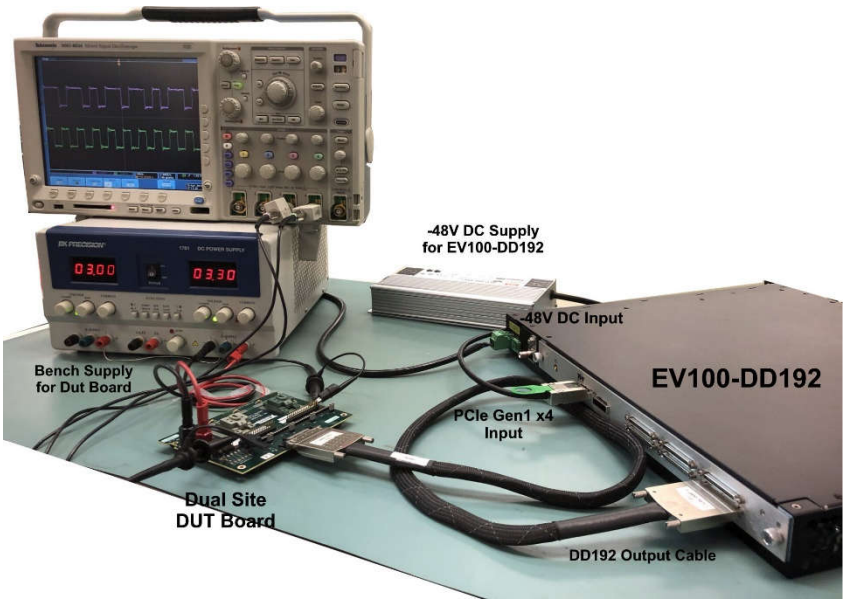
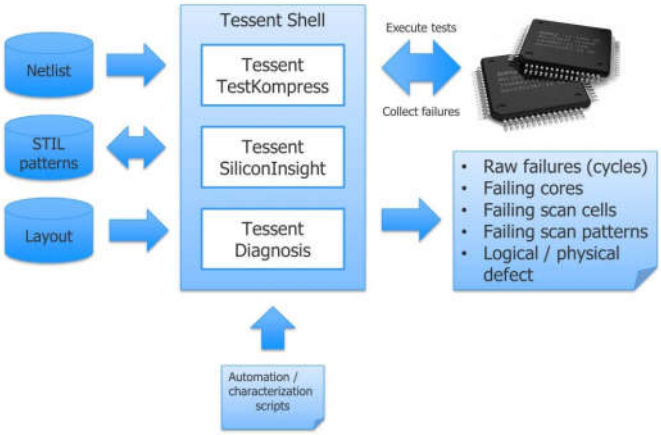


The picture to the left shows an example setup on the lab bench for a two-site DUT board, connected with cables to the EV100 ATE-class digital with built-in deep SCAN pattern dept. Power supplies, and a measurement instruments are also shown in this compact bench setup.

Test time reduction of 15X was observed compared to using an Opal-Kelly board. Device fail data was then cross reference back to the original Tessent SVF pattern. Algorithmic pattern edit capability provides access to device internal registers allowing quick setup for of characterization runs. In addition, porting from an EV100 to other ATE platforms like Teradyne UltraFlex or J750, or Advantest/Verigy 93K is straightforward.

Mentor Tessent

The customer originally used the Mentor Tessent Shell platform to execute the test patterns, and then collect and analyze the fail data. They currently have to switch from the Tessent Shell to the ATE software.



In the future, having the EV100 integration with Tessent Shell would makes it possible for the software to understand how all the test structures and protocols work so that results are returned in a meaningful fashion. When test patterns fail during silicon bring-up, you are typically interested in determining which scan cells capture the failing data. In the presence of on-chip compression and hierarchical DFT, complex decoding and dedicated diagnosis patterns may be required. With this future system, the complex mapping and generation of dedicated diagnosis patterns is now done under the hood, significantly simplifying the debug process.

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About Test Evolution

Test Evolution is a manufacturer of test products, including ATE products for digital, mixed signal and RF test in the AXIe form factor with a range of test systems scaling up to >1000 resources, and MIPI protocol testers for cameras, displays and SoCs using the CSI and DSI standards.

Test Evolution's EV100 series of instruments package high density DC and digital test ATE modules in a convenient 1U module. The instruments follow the AXIe standard providing a single slot cabled solution for Test Evolution AXIe instruments, targeting device characterization as well as production testing. ATE-class test environment software is provided for each instrument, including Instrument Debug and Pattern Debug tools. Mentor Tessent integration is available for lab-based SCAN characterization and debug in the lab.